Altera Quartus II software v9.0 — Subscription Edition vs. Web Edition

Categories	Features	Web Edition software	Subscription Edition software
General information	Getting started	Download (www.altera.com/download) and DVD (www.altera.com/dvdrequest)	
	Operating system support	Windows: Vista (32 bit), XP (32 bit)	Windows: Vista (32/64 bit), XP (32/64 bit) Linux: SUSE Linux Enterprise 9 (32/64 bit), Red Hat Enterprise Linux 4 and 5 (32/64 bit) CentOS 4 and 5 (32/64 bit)
Device support	CPLD	MAX® series devices: All	MAX series devices: All
	Low-cost FPGAs	Cyclone® series devices: All Legacy families: ACEX®, selected APEX II devices	Cyclone series devices: All Legacy families: All
	Midrange FPGAs	Arria® GX FPGAs: All Arria II GX FPGAs: EP2AGX20, EP2AGX30	Arria GX FPGAs: All Arria II GX FPGAs: All
	High-end FPGAs	Stratix® IV / IV GX FPGAs: None Stratix III FPGAs: EP3SE50, EP3SL70, EP3SL50 Stratix II / II GX FPGAs: EP2S15, EP2SGX30 Stratix FPGAs: EP1S10	Stratix IV/ IV GX/IV GT FPGAs: All Stratix III FPGAs: All Stratix II / II GX FPGAs: All Stratix / GX FPGAs: All
	ASIC	No	HardCopy® series: All
IP	Altera and partner IP	Yes, including free OpenCore Plus evaluation feature	
	Full license IP base suite	IP available for purchase	DSP: FIR, FFT, and NCO compilers; Interfaces: SerialLite II; Memory controllers: DDR1/2/3, QDR II, RLDRAM II
Design entry	SOPC Builder	Yes	
	Schematic entry and language support	Schematic entry, Verilog, VHDL, and SystemVerilog	
Design environment	Tcl scripting , command line support	Yes	
Implementation and optimization	Incremental compilation and team-based design	No	Yes
	LogicLock	No	Yes
	Multiprocessor support	No	Yes
	Physical synthesis optimizations	Yes	
	Design space explorer	Yes	
	Chip planner	Yes	
	Live I/O checking	Yes	
	Timing-driven placement	Yes	
	TimeQuest timing analyzer and optimization advisor	Yes	
	Synopsys Design Constraint (SDC) format support	Yes	
	Early power estimator	Available to download on www.altera.com for no cost	
	PowerPlay power analysis and optimization	Yes	
Verification and debug	SignalTap® II logic analyzer	Available with TalkBack enabled	Yes
	SignalProbe feature	Available with TalkBack enabled	Yes
	ModelSim®-Altera Starter Edition	Included	
	ModelSim - Altera Edition	Sold as an option for $945	
	Embedded logic analyzer interface	Yes	
	RTL viewer and technology map viewer	Yes	
	Pin planner	Yes	
System design software	Nios II Embedded Design Suite	Free for both versions of Quartus® II software	
	DSP Builder	Sold as an option for both versions of Quartus II software	
Third-party support	EDA partners	Altera offers third-party support for synthesis, functional and timing simulation, static timing analysis, board-level simulation, signal integrity analysis, and formal verification	

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