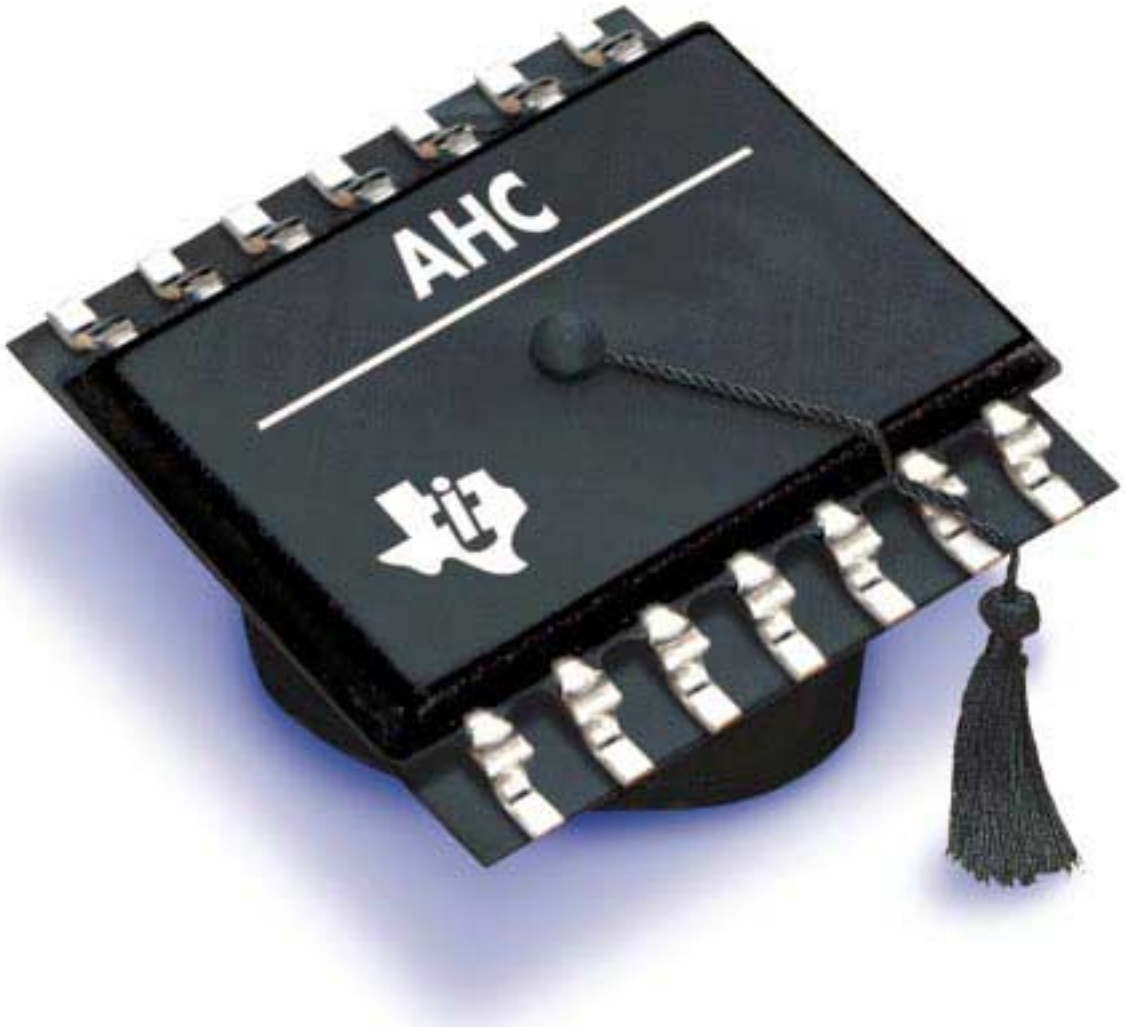
TEXAS INSTRUMENTS

WORLD LEADER IN LOGIC PRODUCTS

AHC/AHCT Designer's Guide

September 1998



Graduate to new performance levels with AHC . . .

- ***3-times faster than HCMOS***
- ***Half the static power consumption of HCMOS***
- ***Same low noise as HCMOS***

. . . for the same market price as HCMOS.

AHC/AHCT
Designer's Guide

SCLA013D
February 2000

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INTRODUCTION

The Advanced High-Speed CMOS (AHC) logic family from Texas Instruments (TI™) provides an effortless migration path for HCMOS users who require higher speed and lower power without paying a noise or price premium. The AHC logic family also offers the broadest selection of logic choices, ranging from simple gates/MSI/octals (SN74AHCxxx) to single-gate (SN74AHC1Gxx) and Widebus™ (SN74AHC16xxx) devices. Add to that the ability to operate at both 3.3 V and 5 V, and you have a reliable migration path from HCMOS.

Performance characteristics of the AHC family are:

- **Low noise** – The AHC family allows designers to maintain the same low noise characteristics of HCMOS without the overshoot and undershoot typical of higher-drive devices usually required to achieve AHC speeds.
- **Low power** – The AHC family, by using CMOS technology, has low power consumption (40-μA maximum static current, one-half that of HCMOS).
- **Speed** – With typical propagation delays of 5.5 ns (’245), AHC offers three times the speed of HCMOS.
- **Drive** – Output-drive current is ±8 mA at 5-V V_{CC} and ±4-mA at 3.3-V V_{CC}.
- **5-V input tolerance at 3.3 V** – With the input diode to V_{CC} removed, AHC is specified for both 5-V and 3.3-V operation.
- **Pin-for-pin compatibility** – All AHC devices are pin-for-pin compatible with industry-standard functional pinouts.
- **Options** – With CMOS- (AHC) and TTL- (AHCT) compatible devices available in gates/MSI/octals, single gates, and Widebus, the AHC family offers the widest selection of logic choices on the market.
- **Packaging** – AHC devices are available in D and DW (SOIC), N (PDIP), DB and DL (SSOP), DGG and PW (TSSOP), DGV (TVSOP), and DBV (SOT) and DCK (SC–70) packages. Selected AHC devices are available in military versions (SN54AHCxx).

For more information on these or other TI products, please contact your local TI representative, authorized distributor, the TI technical support hotline at 972-644-5580, or visit the TI logic home page at http://www.ti.com/sc/logic.

For a complete listing of all TI logic products, please order our logic CD-ROM (literature number SCBC001) or Logic Selection Guide (literature number SDYU001) by calling our literature response center at 1-800-477-8924.

Contents

Contents (Continued)

Your Next Choice: Advanced High-Speed CMOS Logic (AHC)

Speed Up Your System With AHC/AHCT

Do you use HCMOS logic in telecom, computer, industrial, automotive, or consumer applications?

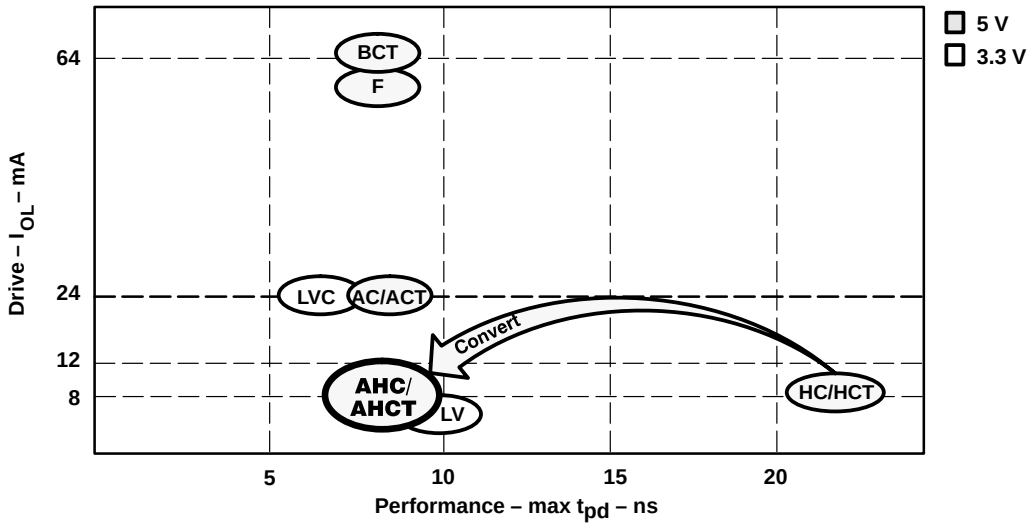
For the same price as HCMOS, would you like to plug in devices with:

- 3-times the speed of HCMOS
- Half the static power consumption of HCMOS
- The same low noise as HCMOS
- A wide supply-voltage range

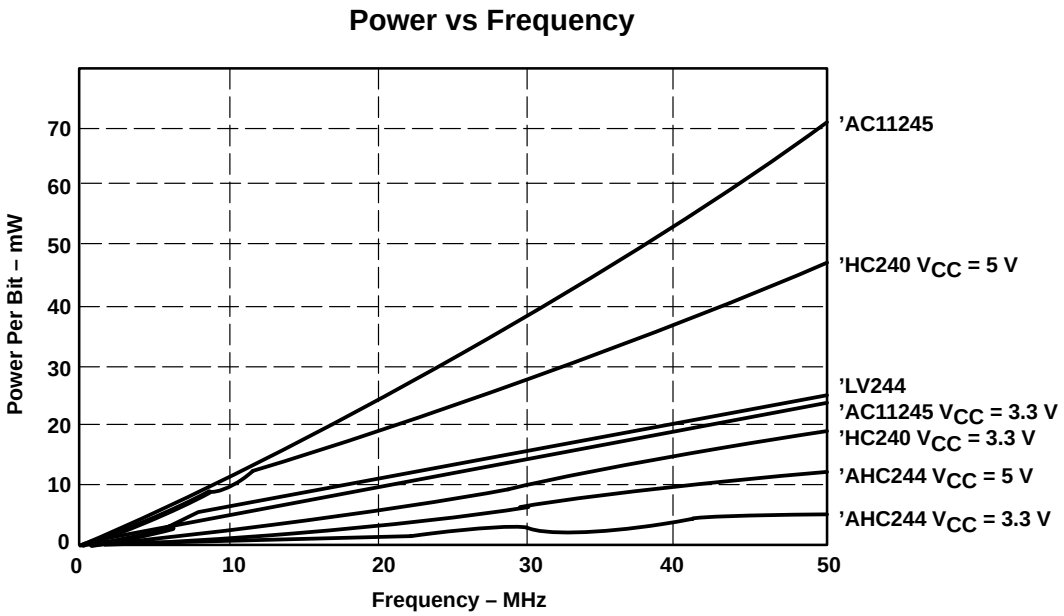
If so, this designer's guide is for you . . . and so is advanced high-speed CMOS (AHC).

Convert HC to AHC

Family Positioning



AC/ACT	Advanced CMOS	HC/HCT	High-Speed CMOS
AHC/AHCT	Advanced High-Speed CMOS	LV	Low Voltage CMOS
BCT	BiCMOS Technology	LVC	Low Voltage CMOS
F	74F Bipolar Technology		



Triple the Speed, Same Drive, But Less Power Consumption

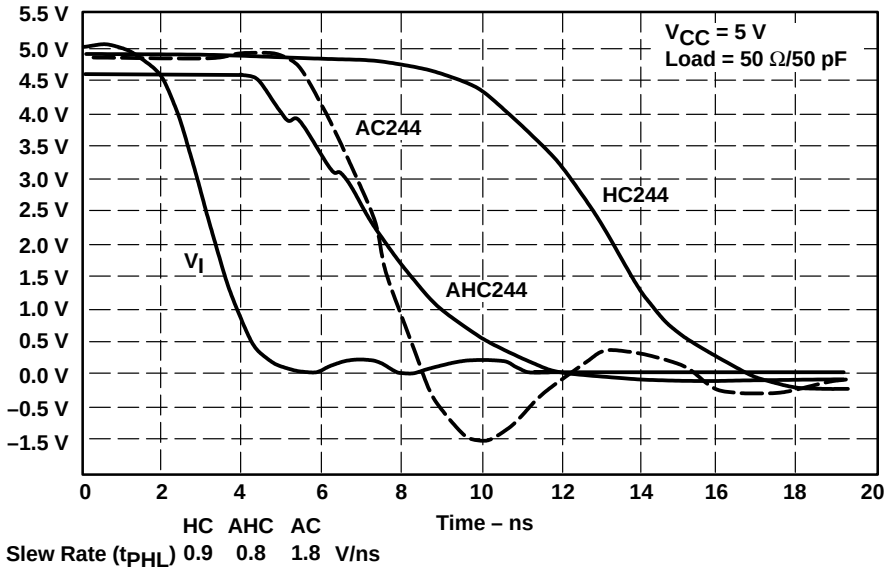
The AHC family typically replaces the slower 5-V HCMOS family, but is additionally specified at V_{CC} = 3.3 V.

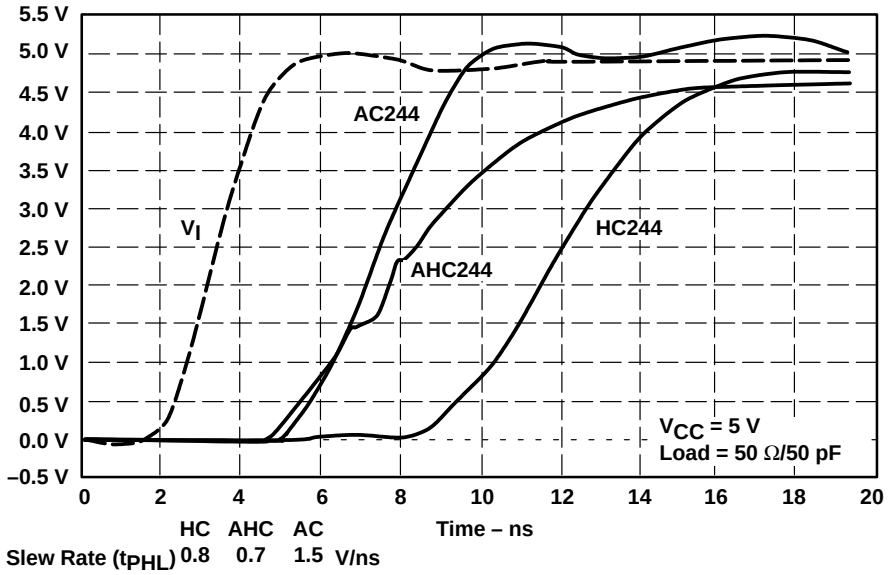
Drive capability is the same as for the HC/HCT family, while speed is comparable to that of the AC/ACT, BCT, and 74F families. For instance, the typical propagation delay time of octal transceiver SN74AHC245 at V_{CC} = 5 V is 5.5 ns (8.5 ns maximum) with drive capability of $I_{OH,OL}$ = ±8 mA. The CMOS-compatible AHC device can be used in low-voltage systems. However, when operated at V_{CC} = 3.3 V, t_{pd} slows to 8.5 ns (typically) at a drive of $I_{OH,OL}$ = ±4 mA.

The comparison of the power consumption between AC, HC, LV, and AHC families shows that for power-critical systems the use of AHC lengthens battery life.

Improve Switching Performance With AHC/AHCT

Switching Characteristics Comparison





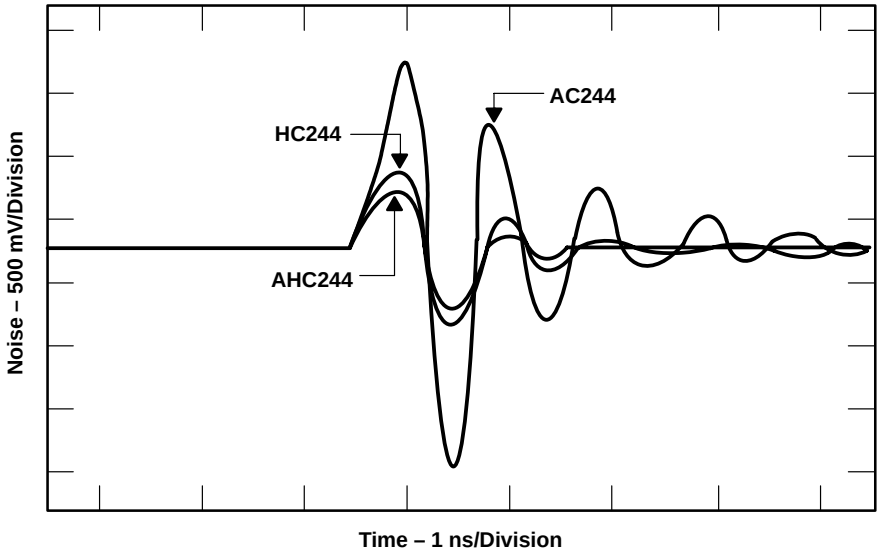
Low Switching Noise

The HCMOS family has very low switching noise, which is achieved primarily through a low slew rate, typically, 0.9 V/ns and the low drive capability of ±8 mA, resulting in low current spikes during switching. Though the speed of AHC/AHCT has been increased, the slew rate of AHC/AHCT is even lower than HCMOS. The ground bounce of AHC devices attributed to simultaneous switching is better than that of the standard HCMOS family. This is specified with the parameters $V_{OL(P)}$ and $V_{OL(V)}$. For example, SN74AHC244:

$V_{OL(P)}$ (typ) = 0.5 V

$V_{OL(V)}$) (typ) = –0.2 V

Ground-Bounce Comparison



Technical Comparison of AHC Versus Other CMOS Logic Families (’245 Function)

		AHC/AHCT		HC/HCT		AC/ACT	
V_{CC}		5 V	3.3 V	5 V	2 V	5 V	3.3 V
Drive		–8/8 mA	–4/4 mA	-8/8 mA	20 μA	–24/24 mA	–12/12 mA
Speed (typical)		5.5 ns	8.3 ns	18 ns	54 ns	3.5 ns	5 ns
Ground bounce		0.5 V (–0.2 V)	N/A	0.6 V (–0.3 V)	N/A	1.5 V (–1.8 V)	N/A
Power dissipation capacitance†		8.6 pF (at 1 MHz)	N/A	40 pF	N/A	45 pF	N/A
Quiescent power dissipation		40 μA		80 μA		40 μA	
Level conversion option	Input	3.3 V	5 V	3.3 V		3.3 V	
	Output	5 V	3.3 V	5 V		5 V	
Widebus package available		Yes	Yes	No	No	No	Yes

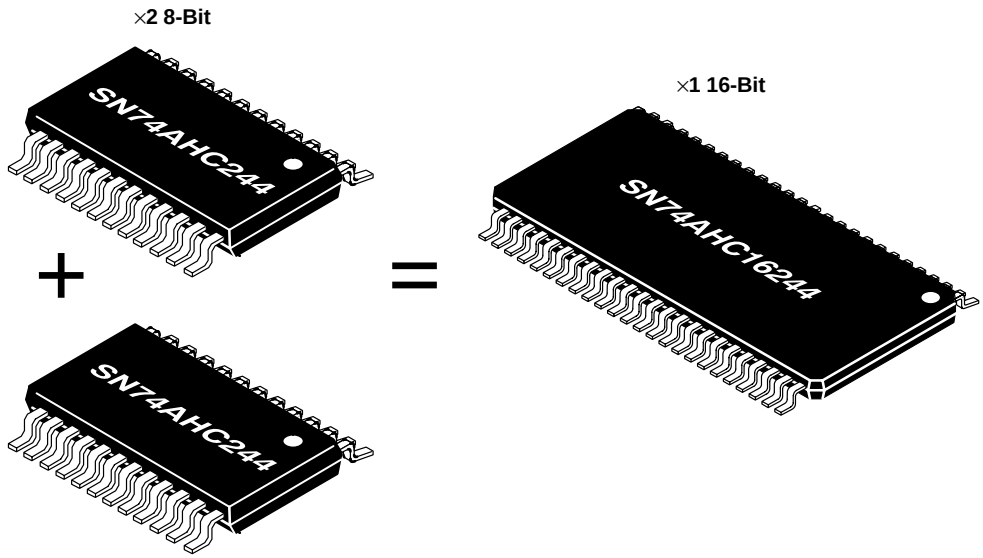
† C_L = 50 pF, f = 10 MHz unless otherwise specified

Widebus Minimizes Board Space (SN74AHC16xxx/SN74AHCT16xxx)

The trend toward 16-bit and 32-bit Widebus systems to increase data throughput continues unabated, requiring bus drivers that support these formats.

Many 16-bit bus systems can be supported easily by TI Widebus devices. These are designed to replace the commonly used 8-bit functions. A single 16-bit Widebus package replaces 2 × 8-bit packages. A typical Widebus example is the SN74AHC16244, which incorporates twice the functionality of an SN74AHC244.

Typical Widebus Example



Multiple Package Options

AHC Packages

	PDIP (N) DUAL-IN-LINE					SOIC (D/DW) SMALL OUTLINE			SOT-23 (DBV) SMALL OUTLINE	SC-70 (DCK) SMALL OUTLINE
PIN COUNT	**14**	**16**	**18**	**20**	**28**	**16**	**20**	**28**	**5**	**5**
Width	6.60	6.60	6.60	6.60	14.22	7.59	7.59	7.59	1.80	1.35
Length	19.69	19.69	23.37	24.77	36.83	10.41	12.95	18.03	3.10	2.2
Pitch	2.54	2.54	2.54	2.54	2.54	1.27	1.27	1.27	0.95	0.65
Height	5.08	5.08	5.08	5.08	5.08	2.65	2.65	2.65	1.3	1.0

	SSOP (DB/DL) SMALL OUTLINE		TSSOP (DGG/PW) SMALL OUTLINE			TVSOP (DGV) SMALL OUTLINE				
PIN COUNT	**20**	**48**	**14**	**20**	**48**	**14**	**16**	**20**	**24**	**48**
Width	5.60	7.59	4.80	4.50	6.40	4.50	4.50	4.50	4.50	4.50
Length	7.50	16.00	5.10	6.60	12.60	3.70	3.70	5.10	5.10	9.80
Pitch	0.65	0.635	0.65	0.65	0.50	0.40	0.40	0.40	0.40	0.40
Height	2.00	2.79	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20

All linear dimensions are maximums specified in millimeters.
All devices comprising gate, flip-flop, or bus functions are available with CMOS- and TTL-compatible I/Os, and are available in a broad range of package options.

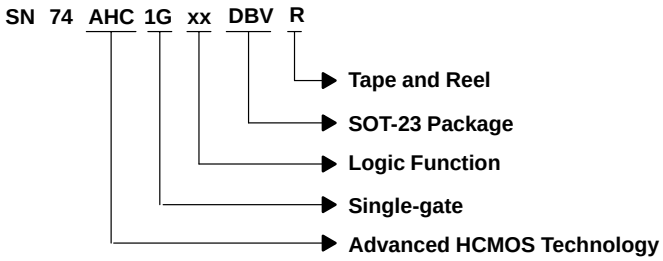
PACKAGES					
	TI NOMENCLATURE	**PHILIPS**	**MOTOROLA**	**FAIRCHILD**	**TOSHIBA**
SOT-23 (new)	DBV (5 pin)	N/A	N/A	M5X	F
SC-70 (new)	DCK (5 pin)	N/A	N/A	P5X	FU
PDIP	N, NT (24 pin)	N	P	N	P
SOIC	D, DW (20 pin–>)	D	M	M	FN
SSOP	DB (24 pin–>), DL (48 pin–>)	DB, DL	SD	MSA, MEA	FS
TSSOP	PW (–>24 pin), DGG (48 pin–>)	PW, DGG	DT	MTC, MTD	ST
TVSOP (new)	DGV (≤ 56 pin)	N/A	N/A	N/A	N/A

Data sheets are available in the *AHC/AHCT Logic Advanced High-Speed CMOS Data Book*, literature number SCLD003A, or at http://www.ti.com/sc/logic.

Single-Gate Logic
(SN74AHC1Gxxx/SN74AHCT1Gxxx)

TI's Single-gate Logic helps designers of handheld systems, such as portable computers, remote control units, and cellular telephones, to reduce the size and weight of their designs. The extremely small logic devices simplify the layout of printed circuit boards, and can be used to make simple functional modifications of ASICs without the cost and delay of redesigning.

Nomenclature

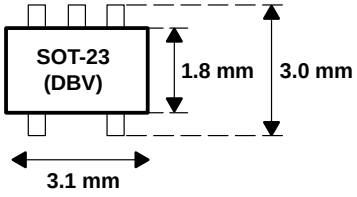


Package

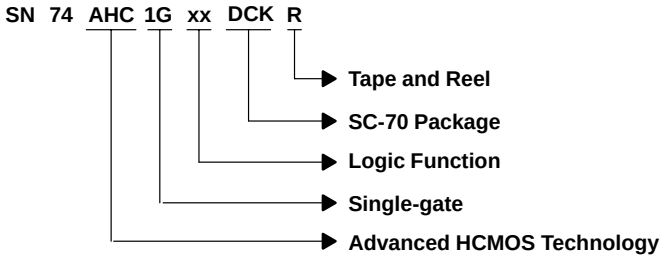
Area: 9 mm^2

Height (max): 1.45 mm

Lead Pitch: 0.95 mm



Nomenclature

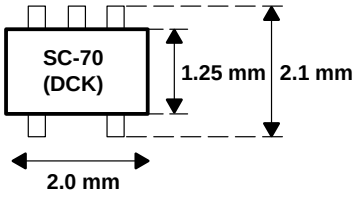


Package

Area: 5 mm^2

Height (max): 1.10 mm

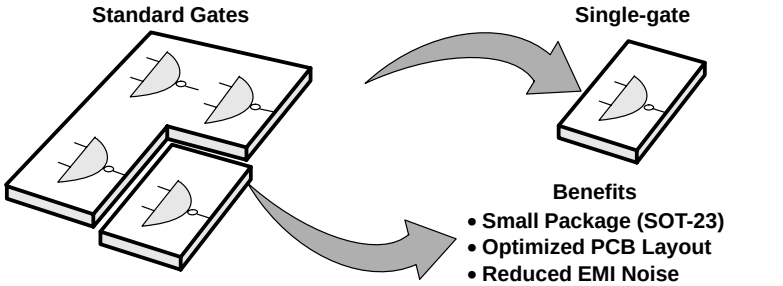
Lead Pitch: 0.65 mm



The Principle

Board Space Comparison

Quad Gate	Single-gate	Area Saving
TSSOP 14 Pin 33.66 mm^2 (max)	SOT-23 5 Pin 9.3 mm^2 (max)	24.36 mm^2 or 72.7%



Benefits

- **Small Package (SOT-23)**
- **Optimized PCB Layout**
- **Reduced EMI Noise**
- **Enhanced ASIC Functionality**

Performance

- 3.5-ns typical propagation delay
- ±8-mA output drive
- 20-µA static current
- CMOS (AHC)- and TTL (AHCT)-compatible versions

Cross-Reference Examples

TEXAS INSTRUMENTS	TOSHIBA
SN74AHC1G00DBV	TC7SH00F
SN74AHCT1G00DBV	TC7ST00F
SN74AHCU1G04DBV	TC7SHU04F

Abstract

With the advanced high-speed CMOS family of logic devices, TI has brought to market a series of components that fully meets today's requirements for increased speed, that is, reduced signal delay time, and for operation from supply voltages of 5 V and 3.3 V. This document first addresses the electrical characteristics of these new devices. A detailed investigation of dc parameters, input/output characteristics, and dynamic behavior follows. Power consumption, cross talk between signal lines, and electromagnetic compatibility also are discussed.

1. Introduction

The introduction of the high-speed CMOS family SN74HC device at the beginning of the 1980s provided the system designer with a sensible and logical alternative to bipolar logic devices, which, until then had been so widely used. These CMOS devices featured delay times approximately comparable to those of the low-power Schottky family. The output currents that these components could deliver were also comparable to those of their bipolar predecessors. An advantage of the CMOS devices is the wide range of supply voltages (2 V to 6 V) with which these components could be operated. It allowed their effective application in battery-operated equipment. However, as with all other CMOS devices, lowering the supply voltage meant that increased delay times had to be tolerated. A few years later, improvements in semiconductor technology made possible the introduction of the advanced CMOS (AHC) devices. In addition to the advantage of a wide range of supply voltage, these devices featured significant improvements in drive capability and delay time. As a result, CMOS devices were for the first time able to penetrate a domain that had been the reserve of fast bipolar logic devices from the SN74F and SN74AS series. Also, whereas CMOS devices were seldom used in applications with extreme requirements of drive capability and speed, such as backplane wiring in large computer systems, advanced CMOS devices established a firm position in all applications. Examples include applications in personal computers and workstations.

With the introduction of notebook computers at the beginning of the 1990s, new requirements were placed on logic devices to perform well at the supply voltage of 3.3 V, which is usual in battery-operated equipment. The HC and AC devices performed inadequately with regard to drive capability and delay time at this low supply voltage. As fast logic circuits, the LVC and ALVC devices were acceptable successors to the AC devices. In drive capability and delay time, these new logic families operating at a supply voltage of only 3.3 V provided the same results as the well-known AC devices using a supply voltage of 5 V. In 3.3-V applications, a useable successor to the HC devices was still missing. In many applications, the outstanding characteristics of the LVC and ALVC devices are not required. In fact, the interference resulting from the steep-edges characteristic of such devices is a disadvantage. They require additional circuit-design precautions, such as multilayer circuit boards, which, in turn, increase equipment costs unnecessarily. With the introduction of the LV series, the attempt was made to create quickly an appropriate logic family. Clever modifications of the process steps in semiconductor manufacturing allowed better performance at a lower supply voltage, but the long-term result was inadequate. Consequently, a new logic family, which, at a supply voltage of 3.3 V, would have the same, or better characteristics as its well-known predecessor was needed. Also, several problems associated with interfaces of circuits operating at 3.3 V and 5 V needed to be addressed. For various reasons, future systems are expected to use both supply voltages.

The logical answer to all these questions is the series of advanced high-speed CMOS devices manufactured in a process that permits gate lengths of 1 μm. The result is typical delay times of 6 ns at 3-V V_{CC} that, in the past, were measured on ALS circuits. This document acquaints the system designer with the characteristics of these advanced components. In addition, a large number of questions with which the designer is often confronted are discussed. Many application problems that can be solved elegantly with this new logic family are shown.

2. DC Characteristics

2.1 Input Circuit

As in all CMOS devices, the input stage consists of a p-channel and an n-channel transistor (see Figure 1) connected in series. With a high logic level at the input ($V_I = V_{CC}$), the n-channel transistor Q2 is conducting and the p-channel transistor Q1 is turned off. A low logic level is created at the output of this inverter. The corresponding complementary state applies with a low logic level at the input ($V_I = 0$ V). In both cases, no current flows through the two transistors. This property is responsible for the low current drain of CMOS devices in the quiescent state.

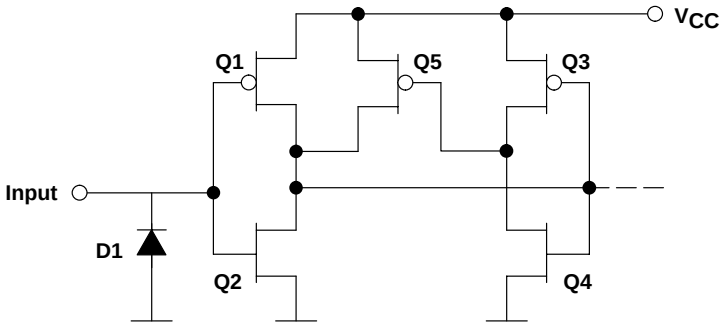


Figure 1. Simplified Input of an AHC Device

Transistors Q1 and Q2 are chosen to have the same transfer characteristics to ensure that the switching threshold of a circuit of this kind is at 50% of V_{CC} (see Figure 2). If the two input transistors Q1 and Q2 have the same characteristics, behavior of the circuit is ensured over a wide range of supply voltage. For CMOS devices, an optimum noise margin is possible in this way. Such devices often are used with interfaces when the other sides deliver only TTL-compatible signals with a high logic level of >2.4 V. To process such signals reliably, a TTL-compatible version with the designation AHCT is available in addition to the AHC family. To shift the switching threshold to lower values, transistors Q1 and Q2 are made so different in their characteristics that the switching threshold becomes about 30% of V_{CC}. Using a supply voltage of 4.5 V to 5.5 V, as is usual with TTL circuits, TTL-compatible threshold voltages for the input stage are achieved (see Figure 3). Such a circuit basically operates with other supply voltages. In this case as well, the threshold voltage has a specific relationship to the input voltage. However, under these conditions the threshold voltage is shifted to values that cannot allow an adequate noise margin in the system. Thus, the TTL-compatible AHCT devices should operate over a range of supply voltage from 4.5 V to 5.5 V.

When a device of this kind is controlled by signals coming from similar devices, and its rise and fall times are only a few nanoseconds, reliable operation can be expected. However, in many cases, for example, at the interfaces with other parts of an equipment, this reliability may not be possible. When there are slowly rising edges at the input, oscillation within the device can occur as a result of high voltage amplification, high cutoff frequency of the transistors, and parasitic components coming mostly from the package (see *Package Construction*). To suppress this oscillator, a kind of Schmitt-trigger circuit has been integrated into the input stage. In addition, the inverted input signal is inverted again with inverter Q3/Q4, and then fed back through transistor Q5 to the output of the input inverter. The switching thresholds on the positive and negative edges at the input differ by about 200 mV and the input circuit has the hysteresis characteristic that is typical of Schmitt-trigger circuits. Transfer characteristics of AHC devices are shown in Figure 2 and those of TTL-compatible AHCT devices are shown in Figure 3.

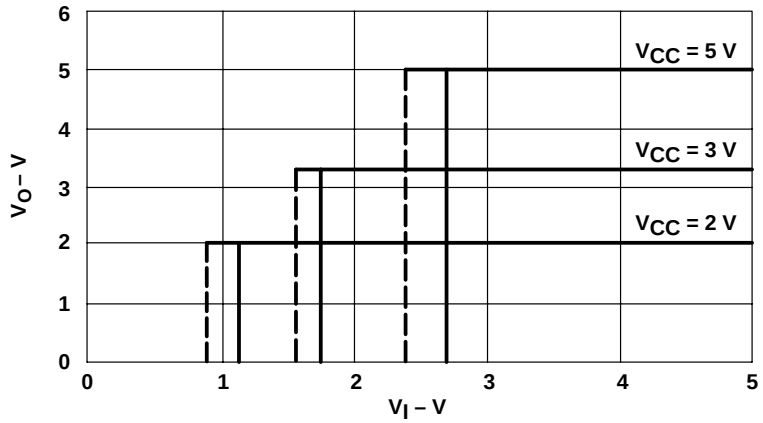


Figure 2. Transfer Characteristics of AHC Devices

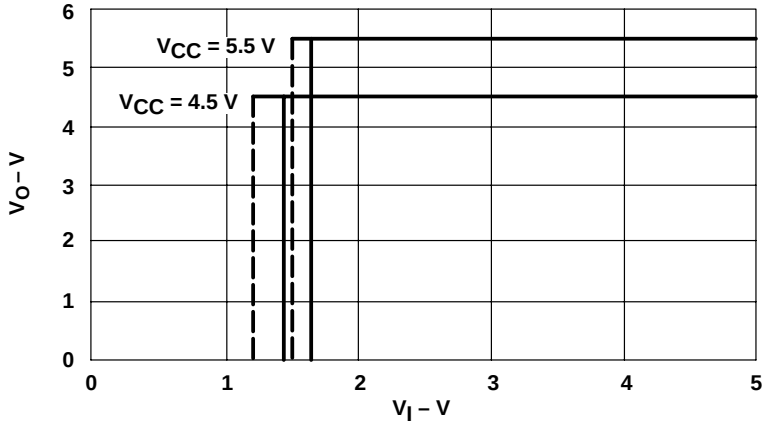


Figure 3. Transfer Characteristics of AHCT Devices

Hysteresis in the input circuit is intended only to process reliably signals that have a slew rate of <10 ns/V. With a signal swing of 5 V, this corresponds to rise and fall times of about 50 ns. If signals with considerably longer rise and fall times are processed, the specially developed Schmitt triggers, such as the SN74AHC(T)14, should be used. These components have a considerably larger hysteresis of about 800 mV at V_{CC} = 5 V and, therefore, allow processing of very slow edges without any problems. When the supply voltage changes, switching thresholds and hysteresis change approximately in proportion to the supply voltage (see Figure 4).

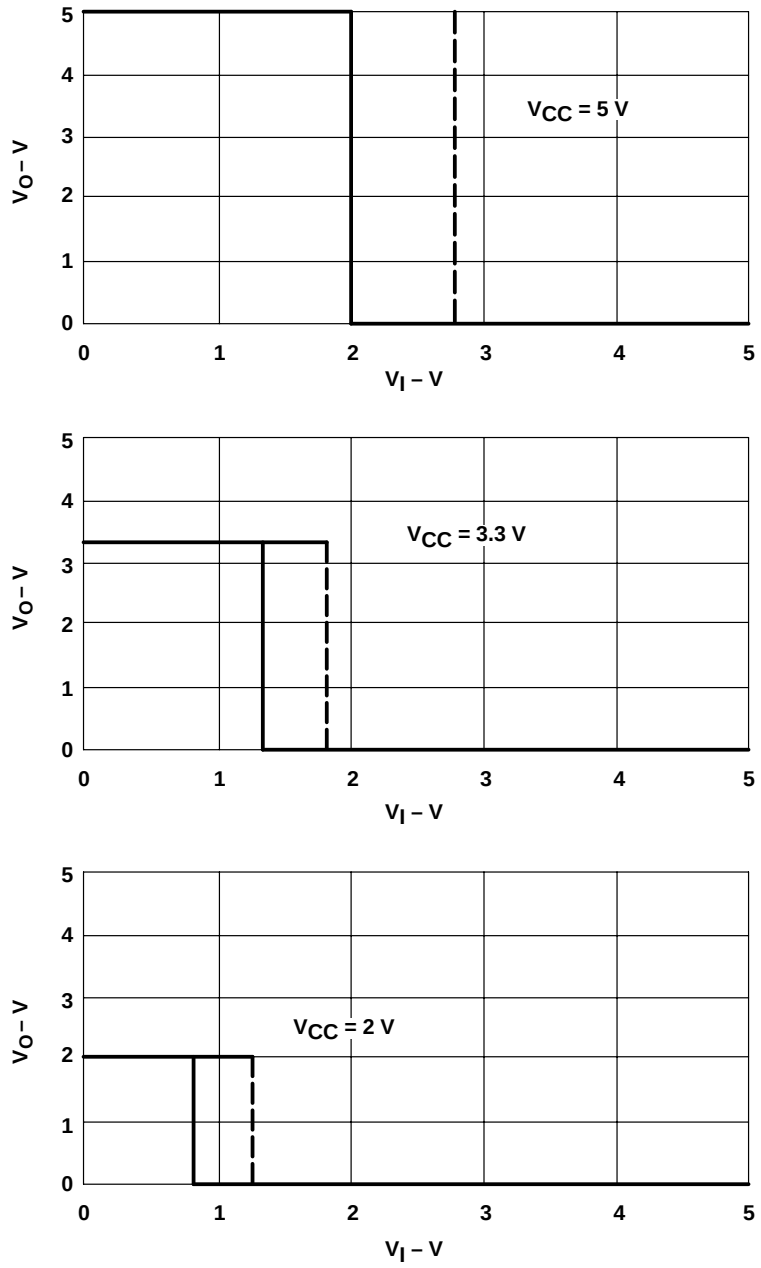


Figure 4. Transfer Characteristics of the SN74AHC14 Schmitt Trigger

To process signals having a swing of only about 3 V in a system with a supply voltage of 5 V, the TTL-compatible SN74AHCT14 Schmitt trigger is available. This device has the same switching characteristics as the previously described Schmitt trigger, except that appropriate circuitry shifts the switching thresholds into the region of the commonly used TTL-voltage levels. Figure 5 shows the transfer function of such components.

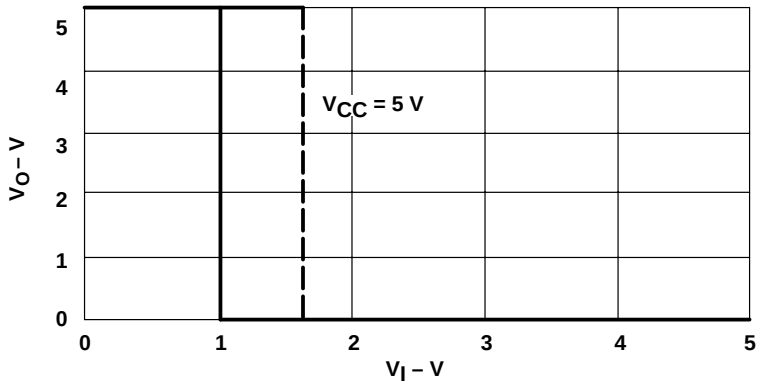


Figure 5. Transfer Characteristics of a TTL-Compatible SN74AHCT Schmitt Trigger

Due to the very low current consumption of CMOS devices in normal operation, only one of the two complementary transistors connected in series conducts. However, this is true only if the input voltage is more negative than the threshold voltage (V_{tn}) of the n-channel transistor or more positive than the supply voltage minus the threshold voltage ($V_{CC} - V_{tp}$) of the p-channel transistor. The threshold voltages V_t of the transistors are, in this case, about 1 V. Over a range of input voltage from $V_{tn} < V_i < (V_{CC} - V_{tp})$, both transistors simultaneously conduct, such that current flows in the input stage that cannot be neglected, and that must be added to the supply current I_{CC} of the circuit. Figure 6 shows the current consumption of AHC and AHCT devices as a function of the input voltage. With both varieties of circuit, the supply current, with the input threshold voltage which is involved, reaches a maximum of about 1 mA to 2 mA. The effective operation of the Schmitt trigger is demonstrated by the transfer characteristics of the AHCT device, as well as in the very rapid change in current that arises after the input voltage exceeds the threshold voltage of ≈1.5 V.

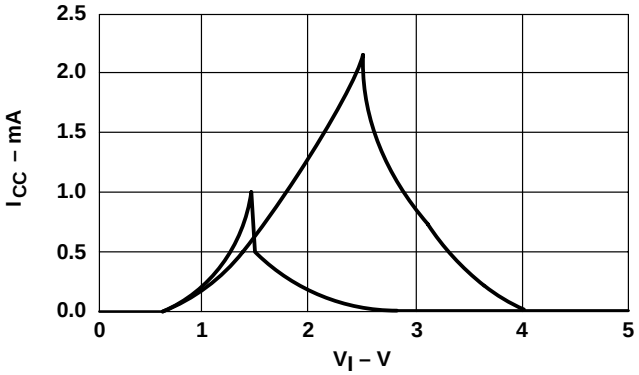


Figure 6. Supply Current as a Function of Input Voltage

In normal operation of a CMOS device, the effect previously described is not relevant, because the high and low logic levels supplied by the outputs of another CMOS device always ensure that the transistor in question turns off. However, if such devices are, for example, controlled by bipolar circuits, results are different. With a high logic level at the output, these supply a voltage that can only be >2.4 V. TTL-compatible CMOS devices, such as those from the SN74AHCT series, recognize such a level as being a high logic state. However, for previously stated reasons, under these conditions a supply current flows in the input stage (see Figure 6), which is significant, particularly with battery-operated equipment. To give system designers specific information about these phenomena, TTL-compatible CMOS-device data sheets have values for the ΔI_{CC} parameter (see Table 1). ΔI_{CC} specifies how much the supply current increases when the high logic level that is typically supplied by a TTL device is applied to one of its inputs. Data sheets show a considerably higher value than that given in Figure 6, but Figure 6 shows only the typical behavior of an AHC or AHCT device. As a result of process and parameter variations and to account for the worst case, values in the data sheets must be used.

Table 1. Specification of ΔI_{CC}

PARAMETER	TEST CONDITIONS		V_{CC}	SN74AHCT245		UNIT
				MIN	MAX	
ΔI_{CC}	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V		1.5	mA

Input characteristics of an AHC device depend on the input of the inverter with a diode connected in parallel (see Figure 1) that is part of the electrostatic discharge (ESD) protection circuit for the input. In addition, the diode limits negative-going overshoots caused by line reflections and improves the quality of the signal. Over a voltage range of $0 \le V_I \le 7$ V, the circuit has an extremely high resistance, as indicated by the value of I_I in Table 2. When a device's output that is in an inactive high-impedance state is connected internally in parallel with an input, as in bidirectional circuits, for example, SN74AHC245, I_{OZ} should be used as the effective input current (see Table 2). The value of I_{OZ} is the sum of the leakage currents of the input and output circuits.

Table 2. Specification of the Input Current

PARAMETER	TEST CONDITIONS		SN74AHC245		UNIT
			MIN	MAX	
I_I	$V_I = V_{CC}$ or GND			±1	μA
I_{OZ}†	$V_O = V_{CC}$ or GND,	$V_{I(OE)} = V_{IL}$ or V_{IH}		±2.5	μA

† The parameter I_{OZ} includes the input leakage current.

Input voltages greater than 7 V must be avoided to preclude damage to the gate oxide of the input stage. This damage is not necessarily permanent, but will adversely affect the expected lifetime of the circuit. The gate oxide of AHC devices is only 200 Å thick. An input voltage of 7 V corresponds to a field strength over the gate oxide of 350 kV/cm. Although breakdown of the oxide is expected only at input voltages above 10 V, electrons tunnel increasingly into the gate oxide at field strengths greater than 350 kV/cm, influencing characteristics of the transistors and causing failure.

In practice, negative input voltages are of greater interest. These voltages result from negative-going overshoots generated by line reflections. To limit these negative overshoots and improve the quality of the signal, an effective clamping diode (D1 in Figure 1) is used. Figure 7 shows a typical input characteristic of an AHC device. The input is at a high resistance with positive input voltages ($0 \text{ V} \le V_I \le 7$ V). With negative input voltages, the clamping diode conducts. It also limits negative-going overshoots at higher currents to voltages of about –1 V (see Figure 7).

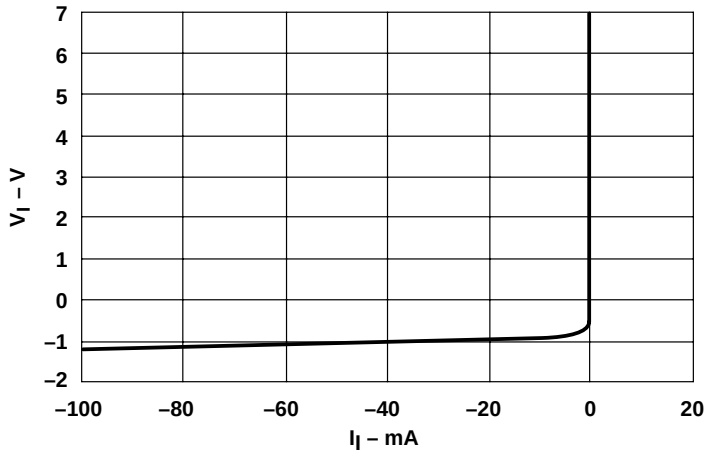


Figure 7. Input Characteristic of an AHC Device

2.2 Output Circuit

The simplified output circuit of an AHC device is shown in Figure 8. Only those components necessary to understand the behavior of the circuit are shown.

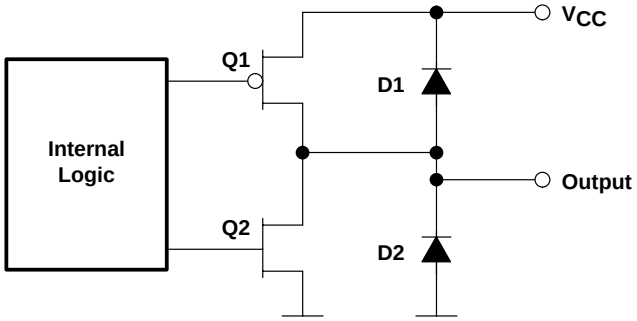


Figure 8. Output of an AHC Device

The internal circuit of the device that drives the load consists of two complementary MOS transistors, Q1 and Q2, connected in series to deliver the necessary output currents. Diodes D1 and D2 are parts of the ESD protection circuit. These diodes, which are created as parasitics during the manufacture of the device, also are intentionally integrated into the internal device circuit. Currents shown in Table 3, which are extracted from the data sheet, are measured under test conditions that produce correct operation of these devices. These values ensure the operation without problems of several logic devices connected together, but give only limited information about their actual behavior.

Table 3. DC Voltage Specifications of the AHC Outputs

PARAMETER	TEST CONDITIONS	V_{CC}	SN74AHC245			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		V
		3 V	2.9	3		
		4.5 V	4.4	4.5		
	I_{OH} = –4 mA	3 V	2.58			
	I_{OH} = –8 mA	4.5 V	3.94			
V_{OL}	I_{OL} = 50 μA	2 V			0.1	V
		3 V			0.1	
		4.5 V			0.1	
	I_{OL} = 4 mA	3 V			0.36	
	I_{OL} = 8 mA	4.5 V			0.36	
I_{OZ}†	$V_O = V_{CC}$ or GND, $V_{I(OE)} = V_{IL}$ or V_{IH}	5.5 V			±0.25	μA

† The parameter I_{OZ} includes the input leakage current.

Figure 9 shows the high- and low-logic output characteristics of AHC devices for various supply voltages. Figure 10 shows the capacitive loading effect on AHC devices.

Output characteristics of AHC devices with 3-state outputs in the inactive high-impedance state are shown in Figure 11. The output data are based on the simplified circuit of the output stage in Figure 8. In the operating state discussed here, output transistors Q1 and Q2 are nonconducting. Over a range of output voltage from $0 V \le V_O \le V_{CC}$, the circuit is, accordingly, at a high resistance. If the output voltage is raised to a value above V_{CC} + 0.7 V, or reduced to below –0.7 V, diode D1 or D2, respectively, conducts and will limit the output voltage. The output characteristic with V_{CC} = 0 V is shown in Figure 11. At this supply voltage, the output transistors do not conduct. The circuit then behaves like two diodes connected in parallel but with opposite polarities. These curves apply to circuits with 3-state outputs and to those with the push-pull output stage, which is usual with all CMOS devices.

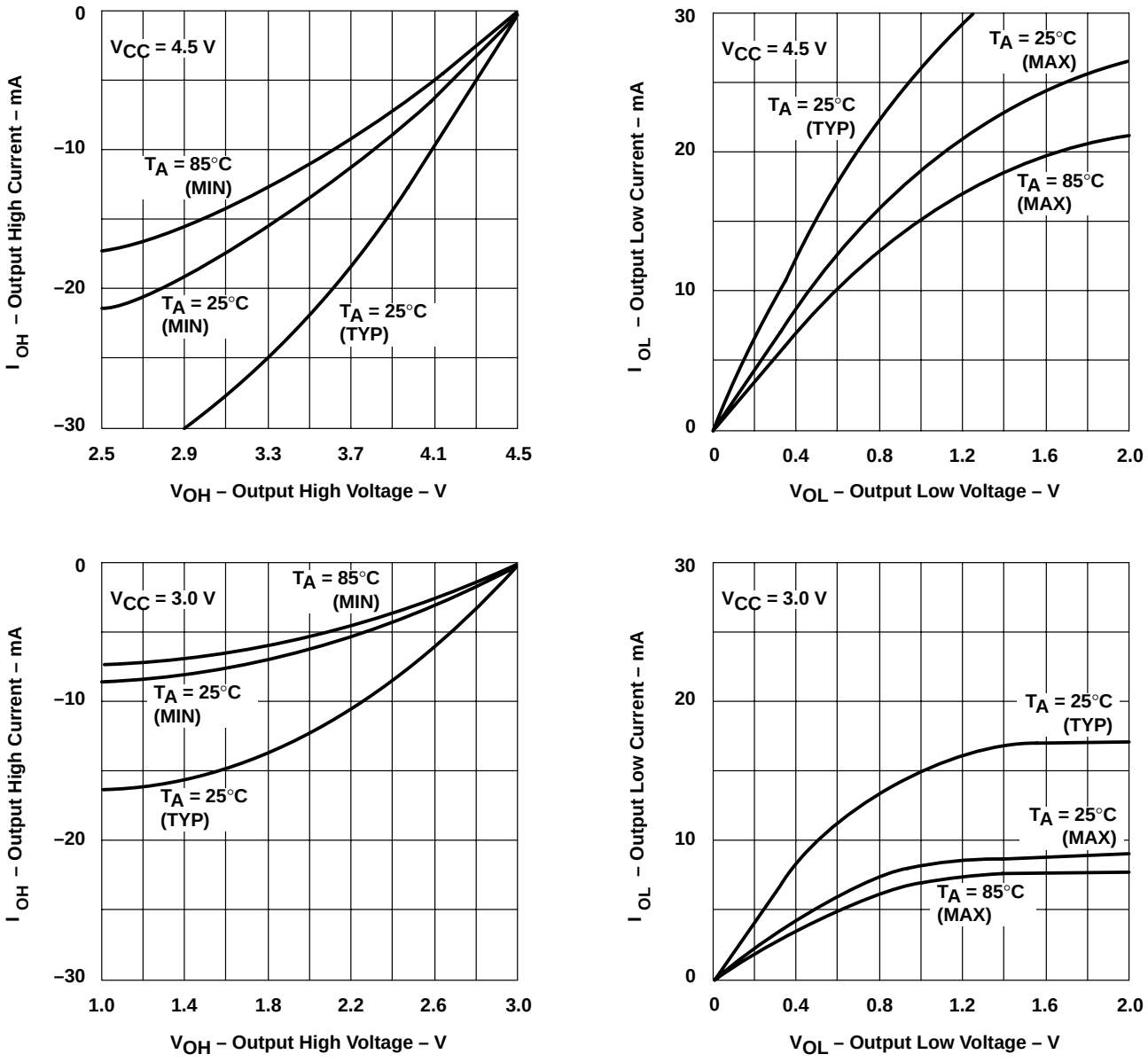


Figure 9. Output Characteristics of an AHC Device

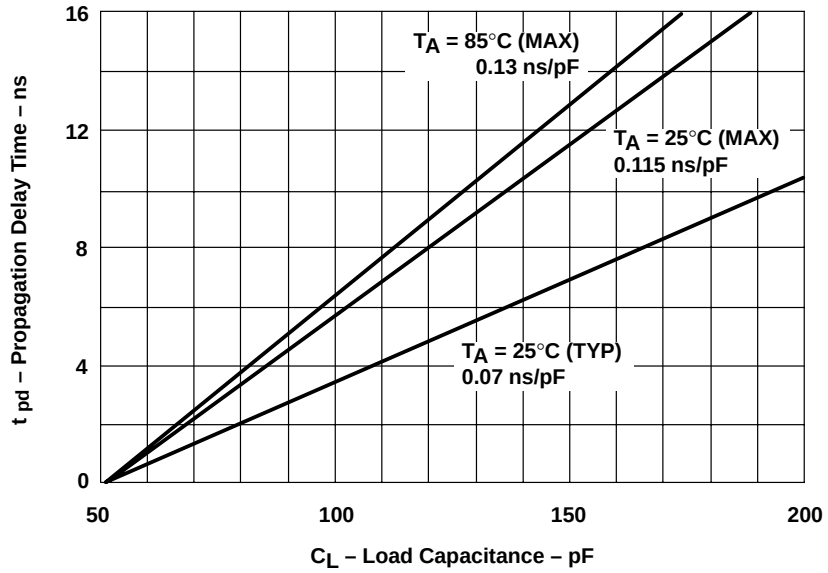


Figure 10. Capacitive Loading Effect on AHC Devices

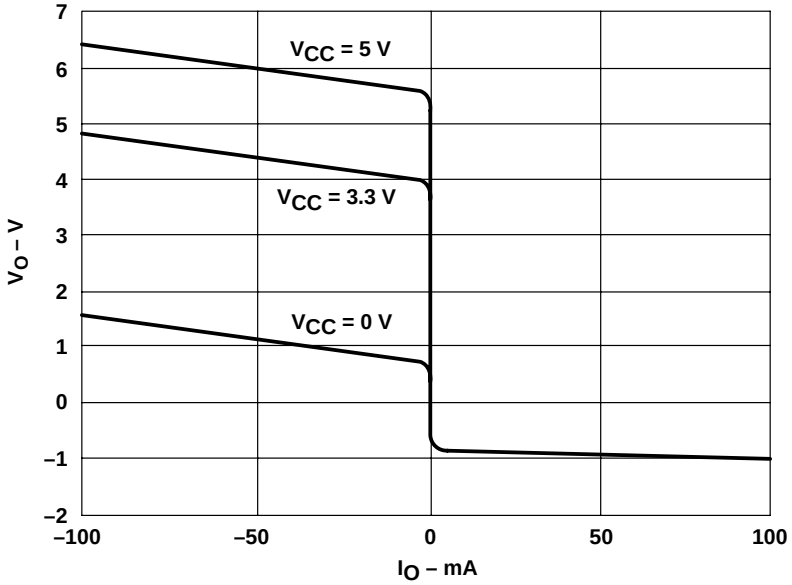


Figure 11. Output Characteristics in High-Impedance State With Supply Voltage Switched Off

2.3 Protection Circuits

Because of their small internal structures, all integrated circuits are susceptible to ESD. An additional problem arises with complementary MOS circuits whose internal structures form parasitic thyristors, which under certain conditions, can be fired and cause a short circuit. Destruction of the device usually is the unavoidable consequence. Therefore, when developing and manufacturing integrated circuits, semiconductor manufacturers must take precautions to protect them from ESD.

2.3.1 Electrostatic Discharge (ESD)

ESD occurs when two bodies with different charges are brought together and an equalization of their charges takes place. This effect is well-known from the situation in which someone walks on a carpet and becomes charged, then touches a metallic object, such as a door handle or water tap. The current that flows as the charge is equalized can be felt as a tingle, or even an unpleasant shock, at the point of body contact. As a result of high charging voltages of several kilovolts and the high currents that result, semiconductors can be destroyed in these circumstances. In practice, three established test procedures reflect the various situations that can arise:

Human-Body Model

This model simulates the situation in which the energy stored in the human body is discharged into the device under test. In this case, a 100-pF capacitor is charged to ±2000 V, then discharged through a resistor of 1.5 kΩ into the device under test. The rise time of the discharge current must be less than a nanosecond.

Machine Model

In this model, immunity to disturbances that contain considerably more energy but have a significantly longer current rise time is tested. For this purpose, a 200-pF capacitor is charged to ±200 V, then discharged without any series resistor into the device under test. The inductances of the lines in the measurement setup (L > 500 nH) reduce the rate of rise of the discharge current sufficiently.

Charged-Device Model

This test simulates the situation in which an integrated circuit is charged, for example, by sliding along a plastic transport rail before insertion by an automatic insertion machine, then is discharged when it touches the printed circuit board. The capacitance of the integrated circuit including package, in which the energy is stored, is then only a few picofarads, but at the instant of the discharge extremely short rise times can be expected. With integrated circuits as currently used, withstanding ±1000 V can be regarded as sufficient in this test.

The engineer who designs integrated circuits must provide protection circuits that will withstand the stresses of the tests described above. A distinction must be made between two destructive processes. High energy levels with relatively long rise times (machine model) in which the protection circuit must be designed with sufficient ability to conduct current away. With the two other test methods, the danger is that, because of the extremely short rise times, the protection circuit will only partially conduct and is overloaded in this region.

Conventional protection circuits consist of diodes or zener diodes that conduct away the currents and limit the voltages. Resistors in series with the circuit to be protected limit the current. Besides reliably diverting the current, whereby the circuit must be protected against thermal overload, the device also must be protected against excessive voltages, for example, to avoid a breakdown of the gate oxide of an MOS transistor. In general, a combination of various methods is used to obtain optimum results.

Figure 12 shows protective circuits used for advanced high-speed CMOS devices. To meet the requirements outlined previously, the protective circuit is constructed in two stages. The input is first protected by a thyristor consisting of transistors Q2 and Q3. This provides coarse protection. If the input voltage rises above about 15 V, transistor Q1 breaks down and fires the thyristor. The latter then short circuits the high currents. Resistors R1 and R2 have values of only a few ohms. Therefore, the holding current of the thyristor is several tens of mA. When the current is reduced again at the end of the discharge, the thyristor is extinguished. Transistors Q4, Q5, and Q6 operate as fine protection and are intended principally to protect the input from excessive voltages. When there are overvoltages at the input, these transistors are driven into breakdown and limit the voltage, while resistor R3 limits the current.

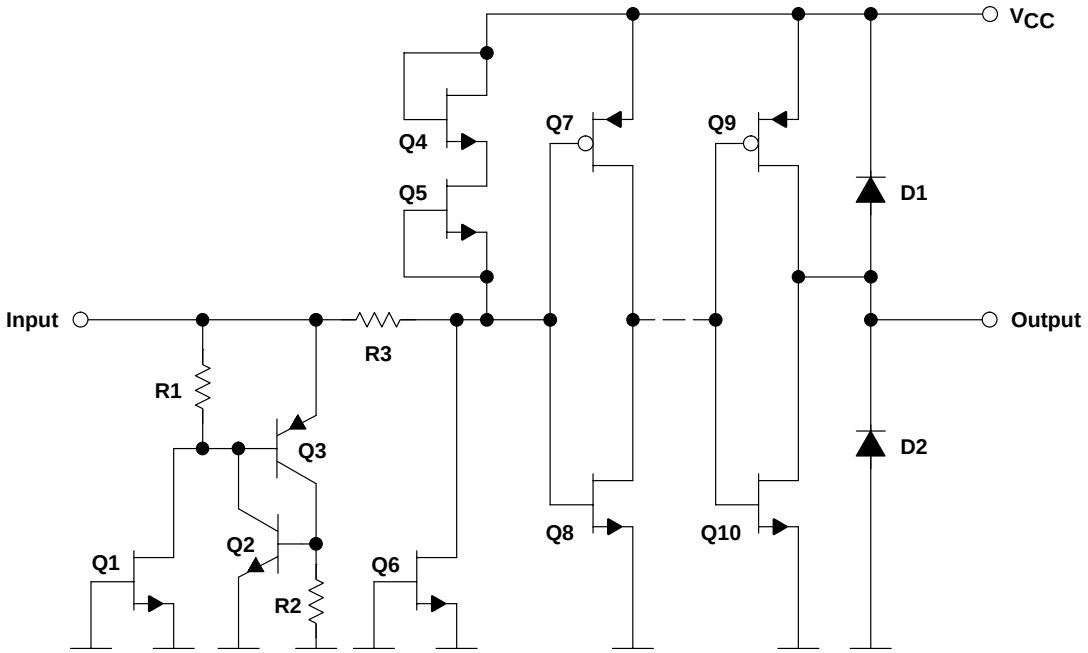


Figure 12. ESD Protection Circuits

A two-stage protection circuit also is to be found at the output of the circuit. The previously mentioned thyristor (Q11, Q12, and Q13) provides coarse protection. Diodes D1 and D2 limit the voltages at the output to tolerable levels.

2.3.2 Latch-Up Protection

When manufacturing complementary MOS circuits, p-n-p-n structures are created internally as a result of the various differently doped regions (see Figure 13). Such structures are thyristors because the anodes and the cathodes are connected to the V_{CC} and GND, respectively, of the integrated circuit, and inputs and outputs of the circuit form the gates of these thyristors. If a sufficiently high current is injected into a termination of this kind, the thyristor fires. A short circuit is produced between the supply-voltage rails, resulting in a high probability that the component will be destroyed.

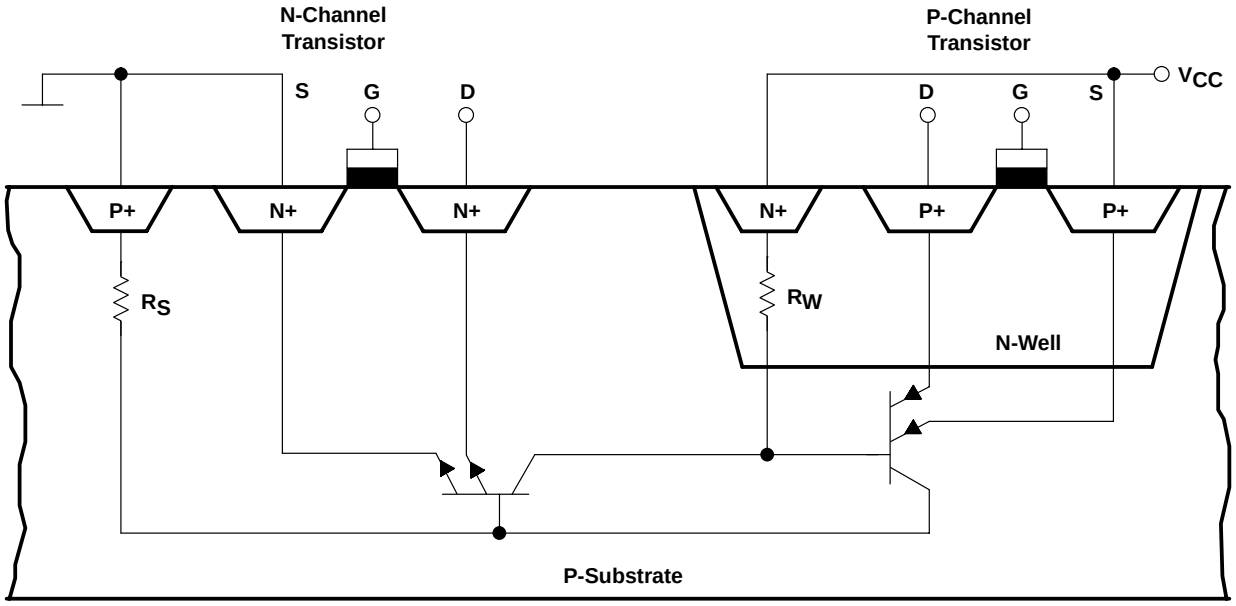


Figure 13. Parasitic Transistors in a CMOS Device

In the early days of CMOS technology, the latch-up effect was a major problem for system designers. Often, many additional precautions had to be taken in a system to avoid excessive currents in the connections to integrated-circuit devices. This inevitably increased the cost of the complete equipment. To counteract the disadvantage of CMOS devices at that time, precautions were taken later when designing the device to prevent latch-up from occurring. This began with the choice of a high-resistance substrate to prevent the spreading of undesired currents. In addition, n- or p-doped guard rings (see Figure 14) were placed around critical parts of the circuit that were connected to the corresponding supply-voltage rails. These guard rings function as additional collectors of the parasitic transistors. Since these collectors are considerably closer to the corresponding base-emitter areas than the bases of the complementary transistors, they take the major part of the current that wanders about in the substrate. In this way, the thyristor is not completely eliminated. However, its sensitivity is reduced to such an extent that, under normal operating conditions, triggering the thyristor is not expected. During the characterization of a new component (type testing), its resistance to latch-up also is checked. With AHC circuits, a current of ±300 mA is applied to all relevant pins of the device under test. At an ambient temperature of 125°C and V_{CC} = 7 V, latch-up must not occur. At room temperature, currents of more than 1 A typically are necessary to cause latch-up.

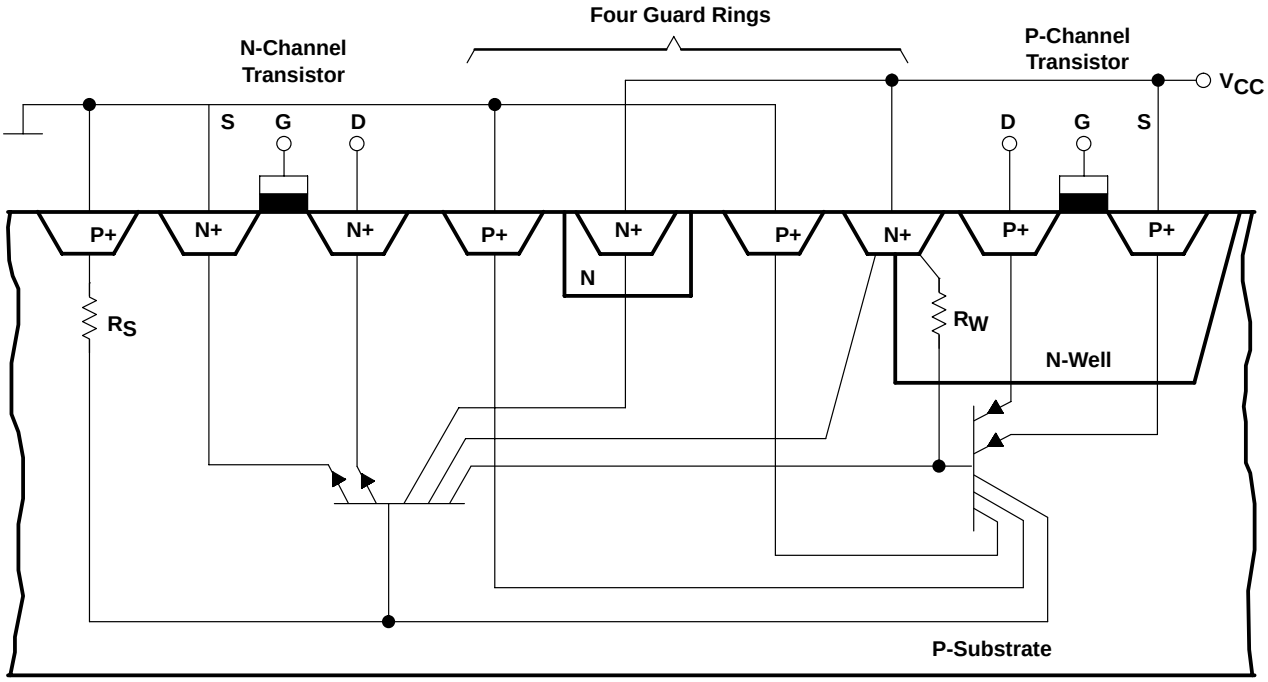


Figure 14. Guard Rings in a CMOS Device

3. Dynamic Behavior

An important parameter when choosing a device is the delay time. Table 4 gives a comparison between HC/HCT and AC/ACT devices. Advanced high-speed CMOS devices are about three times faster than comparable HC devices; AHC and the TTL-compatible AHCT devices have only minor differences with regard to their dynamic characteristics.

Table 4. Comparison of the Delay Times of HC and AHC Devices

DEVICE	SN74HC	SN74HCT	SN74AHC	SN74AHCT
'244 buffer	13 ns	15 ns	5.8 ns	5.4 ns
'245 transceiver	15 ns	14 ns	5.8 ns	4.5 ns
'373 latch	15 ns	20 ns	5 ns	5 ns
'374 flip-flop	17 ns	25 ns	5.4 ns	5 ns

3.1 Power Dissipation

The power dissipation of a CMOS circuit is made up of three distinct components:

- Quiescent power dissipation, P_r
- Internal switching losses, P_S
- Losses P_l, that result from the load connected to the output

The following expression thus applies:

$$P_{ges} = P_r + P_s + P_l \quad \textbf{(1)}$$

The quiescent power dissipation, P_r, is calculated as the product of the supply voltage, V_{CC}, and the quiescent current, I_{CC}, as given in the data sheet. This quiescent current results primarily from the leakage currents of the reverse-biased p-n junctions in the integrated circuit. At room temperature, it is only a few nanoamperes. This current usually can be neglected, but leakage currents in depletion layers typically double with a temperature increase of 10°C. In equipment that is operated at high temperatures, this leakage current can be significant.

The switching loss, P_S, results from charging, discharging, and switching processes inside the device. The charge and discharge of the internal capacitances of the circuit make up a minor part of the total. The major part comes from the current spikes that occur when switching every CMOS stage and which, in this case, primarily affect the output stage. If a CMOS output stage (shown in Figure 8) is switched from a high to low logic level or vice versa, the control voltage on the gate of the transistor within the device only rises (or falls) in a finite time from low to high. The complementary transistor also is being driven in this finite time. Thus, at the moment of switchover, both transistors conduct simultaneously for several nanoseconds. Therefore, a considerable current flows for a short time (see Figure 15) in the circuit. When measuring this current, care must be taken not to capacitively load the output being measured.

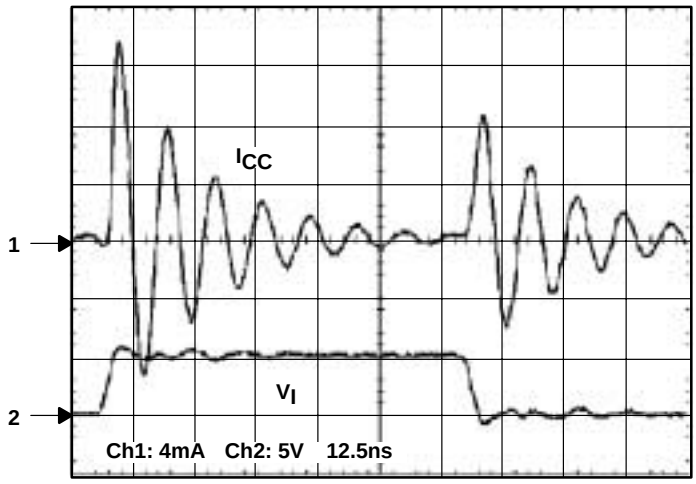


Figure 15. Current Spikes When Switching an AHC Output

The charge, Q, and the energy consumed can be calculated at every switching cycle from the amplitude of the current and its waveform over a period of time. In this way, switching loss, P_S, can be calculated. In practice, a simpler process is used. The supply current, I_{CCS}, of the circuit being considered is measured at a specific input frequency, f_I, but the output must not be loaded. This current consumption can be thought of as generated by an equivalent power-dissipation capacitance, C_{pd}, at the output of the circuit. The following expression then applies:

$$I_{CCS} = C_{pd} \cdot V_{CC} \cdot f_I \quad \textbf{(2)}$$

or

$$C_{pd} = \frac{I_{CCS}}{V_{CC} \cdot f_I} \quad \textbf{(3)}$$

This power-dissipation capacitance, C_{pd}, is given in the data sheet. In a particular application, the following formula can be used to calculate the switching loss P_S:

$$P_s = C_{pd} \cdot V_{CC}{}^2 \cdot f_I \quad \textbf{(4)}$$

Where:

V_{CC} = Supply voltage (V)
f_I = Input frequency (Hz)
C_{pd} = Power-dissipation capacitance (F)

For circuits with 3-state outputs, such as the SN74AHC244, two C_{pd} values are given. One is for the case in which the output is active, and the other for the case in which the output is in the inactive high-impedance state.

The third component of the total power dissipation, P_{ges}, is contributed by the charging and discharging of the load connected to the output. The simplified assumption is that the load connected consists of a capacitor, C_L. The power dissipation, P_l, resulting from this load can be calculated as follows:

$$P_I = C_L \cdot V_{CC}{}^2 \cdot f_O \quad \textbf{(5)}$$

Neglecting the quiescent power dissipation, P_r, the following expression gives total power dissipation:

$$P_{ges} = \left(C_{pd} \cdot f_I + C_L \cdot f_O\right) V_{CC}{}^2 \quad \textbf{(6)}$$

For a SN74AHC244, the data sheet gives a power-dissipation capacitance, C_{pd}, of 8.6 pF. With a capacitive load, C_L, of 50 pF and V_{CC} = 5 V, the following then applies:

$$P_{ges} = (8.6\ \text{pF} \cdot f_I + 50\ \text{pF} \cdot f_O)5^2 \quad \textbf{(7)}$$

With a buffer such as the SN74AHC244, the input and output frequencies are the same ($f_I = f_O$). In this case, the resulting power dissipation per output becomes:

$$P_{ges} = 1.47\ \text{mW/MHz} \quad \textbf{(8)}$$

Figure 16 provides a comparison between the theoretical power dissipation calculated from the formula above and the dissipation actually measured. There is good correlation between the theoretical result and the measurements made. Figure 17 shows the measurement results at a supply voltage V_{CC} = 3.3 V and load of 50 pF or with no load at the output.

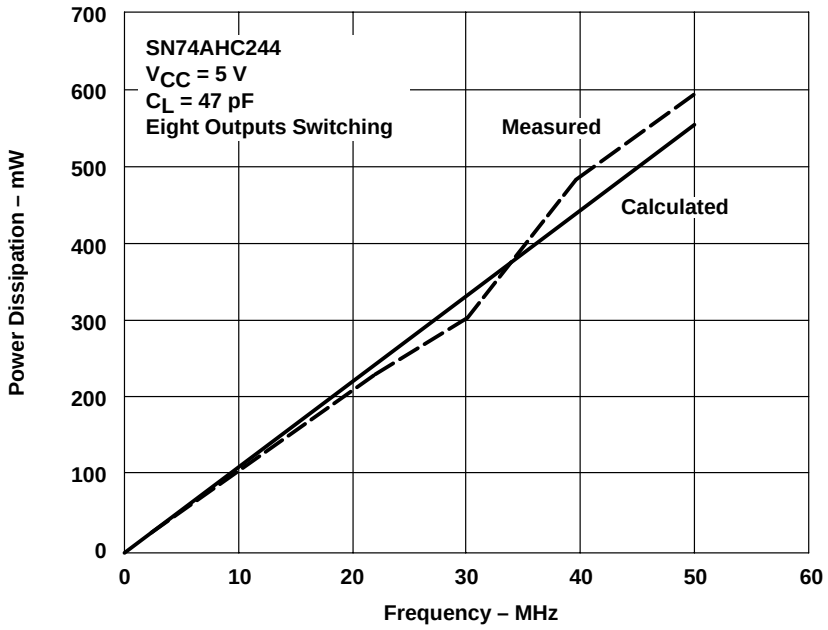


Figure 16. Power Dissipation of SN74AHC244 Bus-Interface Device (V_{CC} = 5 V)

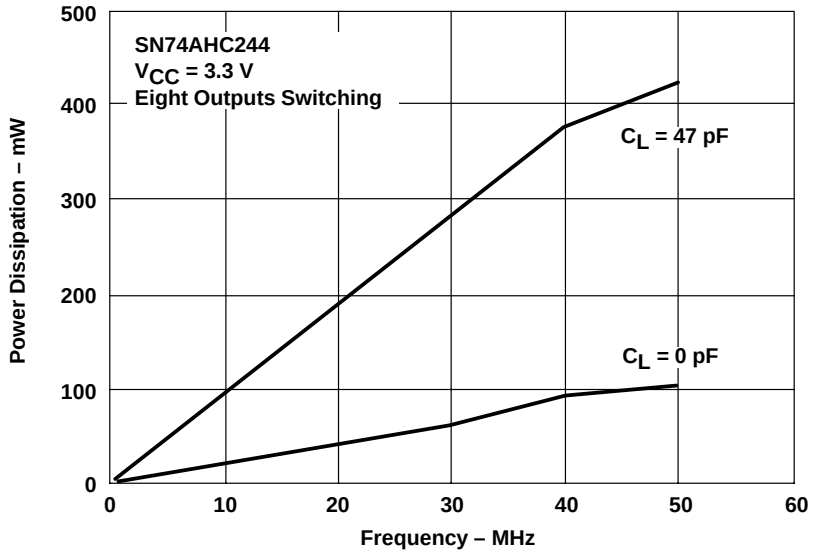


Figure 17. Power Dissipation of SN74AHC244 Bus-Interface Device (V_{CC} = 3.3 V)

3.2 Quality of the Waveforms

An important parameter that significantly affects a circuit or system is the quality of the waveforms. The signals transmitted by the output of an integrated circuit are influenced in many ways en route to the receiver. One form of interference is cross talk, which is coupled from nearby lines to the line where the transmission is occurring. With fast logic circuits, additional interference is generated within the circuits themselves, which can be traced back to the voltage drops across the inductances of the package. Last, waveform distortions occur as a result of reflections along the line.

3.2.1 Cross Talk

The cross talk between adjacent signal lines results from the undesirable inductive and capacitive coupling between them. A precise mathematical treatment of this phenomenon is very complicated, particularly because the precise electrical characteristics of the lines, such as the line inductance and capacitance and the line mutual inductance and mutual capacitance, must be known. For the system designer, it usually is sufficient to know the behavior of typical configurations to draw conclusions about similar situations in other applications. Typical line configurations are illustrated in Figure 18.

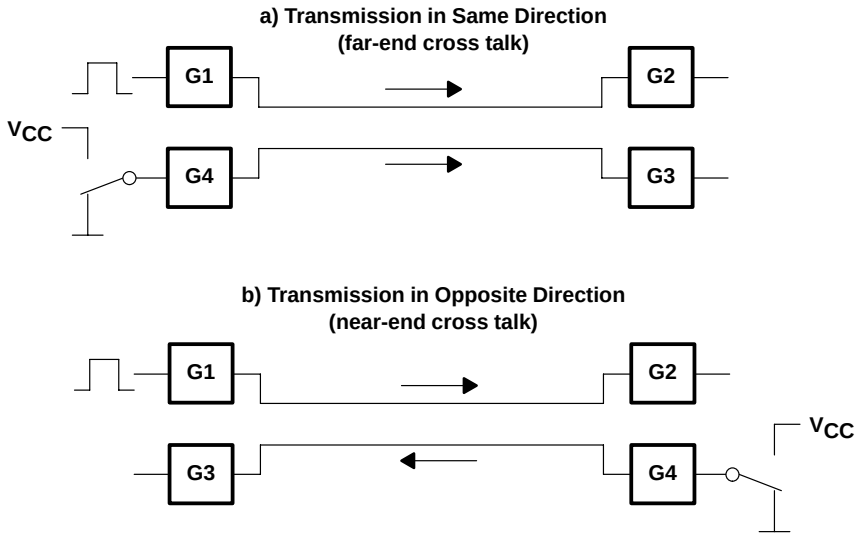


Figure 18. Power Transmission in Same and Opposite Directions

For the following measurements, a measurement setup was used in which on a circuit board two 0.6-mm wide, conductors with a spacing of 0.6 mm were run parallel over a distance of 25 cm. Experience has shown that significantly different results are not obtained with a narrower conductor width, provided the ratio of conductor width to conductor spacing is 1:1.

If gate G1 is switched to have transmission in the same direction (see Figure 18a), the change of voltage is coupled inductively and capacitively into the line running parallel with it. The interfering signal first encounters the low resistance output of gate G4, where it is largely short circuited. After the waveform arrives at the end of the line subjected to this interference, only a low level of interference voltage will be measurable at the input of gate G3 (see Figure 19). With respect to cross talk, this configuration, known as far-end cross talk, is not critical.

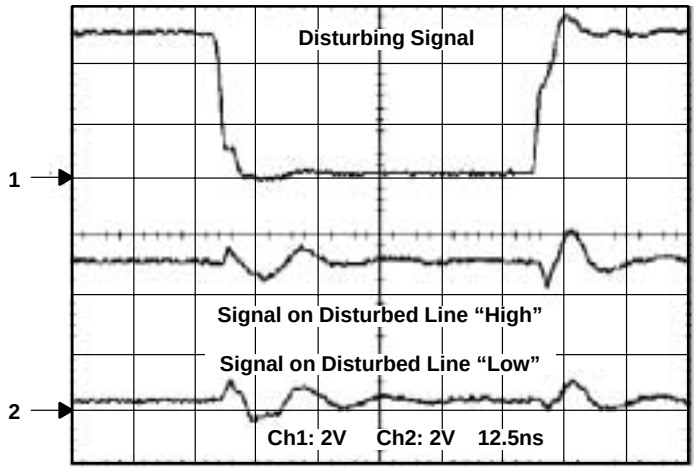


Figure 19. Far-End Cross Talk With Line Length of 25 cm

The behavior is different with transmission in opposite directions (see Figure 18b). The interfering signal, which is coupled into the disturbed line when gate G1 is switched, encounters the high-resistance input of G3 and has significant effects. The disturbance then runs to the end of line G3–G4 (output at G4). Because the output impedance of this gate typically is significantly lower than the line impedance, the interfering waveform is reflected with reversed polarity. After its return, the disturbance will arrive at the input of gate G3. At this point, an interfering pulse can be expected, the length of which is determined as a result of its doubled signal propagation time on this line. Line length directly influences the magnitude of the interference. This considerably more critical manifestation of cross talk is known as near-end cross talk. In the example shown, AHC devices should not have been disturbed. Their switching threshold is typically about 2.5 V, providing an adequate noise margin. In contrast, the situation is different when G3 (see Figure 18b) has a TTL-compatible input stage with a threshold voltage of 1.5 V. In this case, the switching threshold of the circuit that is disturbed is clearly exceeded and experience has shown that this can lead to false triggering. As mentioned previously, the length of the interference pulse, t_w, is in accordance with the doubled signal propagation time on the line in question. With a line having a length of 25 cm and a typical signal propagation time of 6 ns/m (see Figure 20), the width of the resulting interference pulse is:

$$t_w = 2 \cdot t_p \cdot l = 2 \cdot 6\frac{ns}{m} \cdot 25\ cm = 3\ ns \quad \textbf{(9)}$$

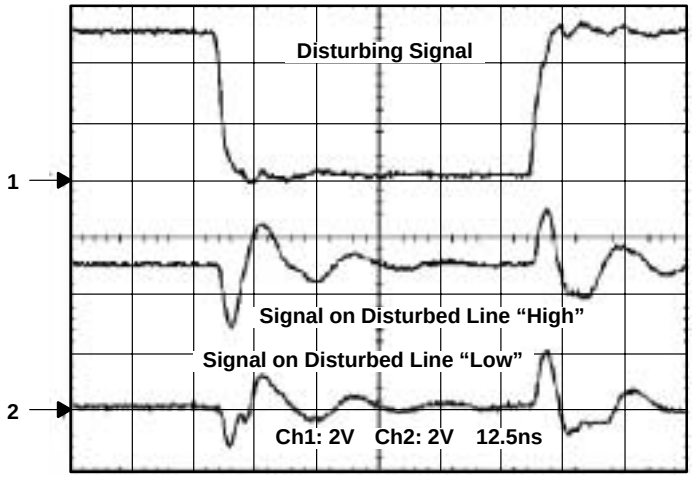


Figure 20. Near-End Cross Talk With Line Length of 25 cm

There are various ways to reduce cross talk between signal lines. One method is to shorten the length of signal paths. In most cases, this will solve the problem because most connecting paths on circuit boards are significantly shorter than 25 cm. With a line length of 12 cm, which covers the majority of connections on circuit boards, signal propagation time, t_p, is 0.75 ns; thus, the width of the interference impulses, t_w, that can be expected is 1.5 ns. Under these conditions, at least as far as cross talk is concerned, there should be no more problems. Also, with appropriate construction of the circuit board, the coupling between the signal lines can be reduced. One precaution consists of incorporating a continuous ground plane under the signal lines. This usually is achieved by correct construction of multilayer circuit boards. With these boards, supply voltage layers (V_{CC} and ground), which lie directly over one another, reduce disturbances on the supply voltage rails and produce significantly less cross talk.

As shown in Figure 21, screening between critical lines provides a significant improvement in every case. For these measurements, an additional ground line having a width of 0.6 mm was placed between the signal lines. As a result of the reduction of the undesired coupling, the amplitude of the coupled signal was reduced. With construction of this kind, transmission over considerably greater distances also is possible. Having a ground layer under the signal lines and a signal-return ground line beside the signal line significantly improves the electromagnetic compatibility of the circuit. Both precautions reduce the area of the effective antenna. In this way, the danger of undesirable radiation of electromagnetic energy and the sensitivity of the circuit to radiation from outside is reduced.

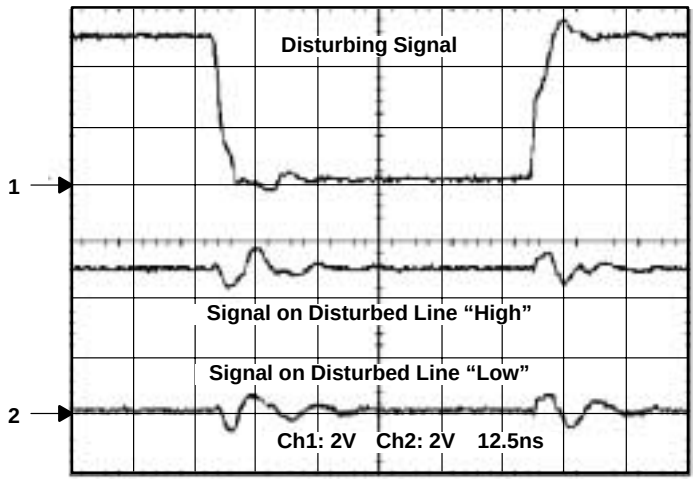


Figure 21. Near-End Cross Talk With Screening Between the Lines and Line Length of 25 cm

3.2.2 Ground Bounce

Shifts of the ground potential (ground bounce) can have various causes. They can result from voltage drops across the ohmic resistance of the ground connections of a circuit. These dc voltage drops can be neglected in most cases. The situation is different with voltage drops that result from rapid current changes in the inductances of the lines. The inductances of the connections within an integrated circuit have significant implications for proper operation of the device. If one or more outputs in an integrated circuit are switched simultaneously, voltage drops on the supply voltage connections can influence the potential at an output that is not involved. The expression used in this case is simultaneous switching noise interference as a result of switching several outputs at the same time.

This behavior can be explained in more detail by referring to the circuit in Figure 22. The input of inverter Q1/Q2 is switched from a low to a high logic level while the input of inverter Q3/Q4 is at a high logic level. The current that flows when discharging capacitor C1 results in a voltage drop across inductances, L_g, of the connections within the package, in this case, primarily the inductance of the ground connections. This raises the internal ground potential of the integrated circuit. This change of voltage can be calculated using the following formula:

$$\mu = L \cdot \frac{di}{dt} \quad \textbf{(10)}$$

It is this change of voltage that appears with undiminished amplitude at the output of inverter Q3/Q4, and the output potential should remain constant. Circuits connected to its output may be influenced by this disturbance. The same effect, but with opposite polarity, occurs when the output in question is at a high logic level and the other outputs of the circuit are switched from a low to a high logic level.

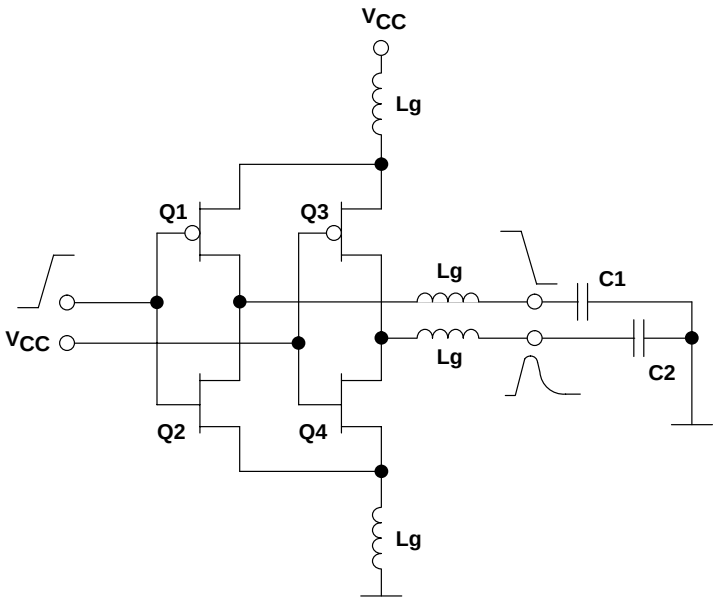


Figure 22. Formation of Shifts of Ground Potential

The interference voltage that can be expected at an output that is in a quiescent state is proportionately higher as the number of outputs that switched simultaneously is increased. These disturbances commonly are known as simultaneous-switching noise, and only devices that can switch several outputs simultaneously are affected. Of principal interest are bus-interface circuits with 4, 8, 16, and even 20 outputs. To evaluate these effects, the measurement setup in Figure 23 has proven to be most effective. With an n-channel circuit, n – 1 outputs are driven simultaneously, while the remaining outputs stay in a quiescent state. All outputs have a 50-pF load (load capacitance includes probe and jig capacitance). This capacitance has proven to be a good choice. Smaller capacitors are not recommended because they would be charged and discharged so rapidly during the switching process that the current could not reach its maximum value. Conversely, capacitors larger than 50 pF do not give rise to any higher currents because currents are limited by the drive capability of the circuit under investigation.

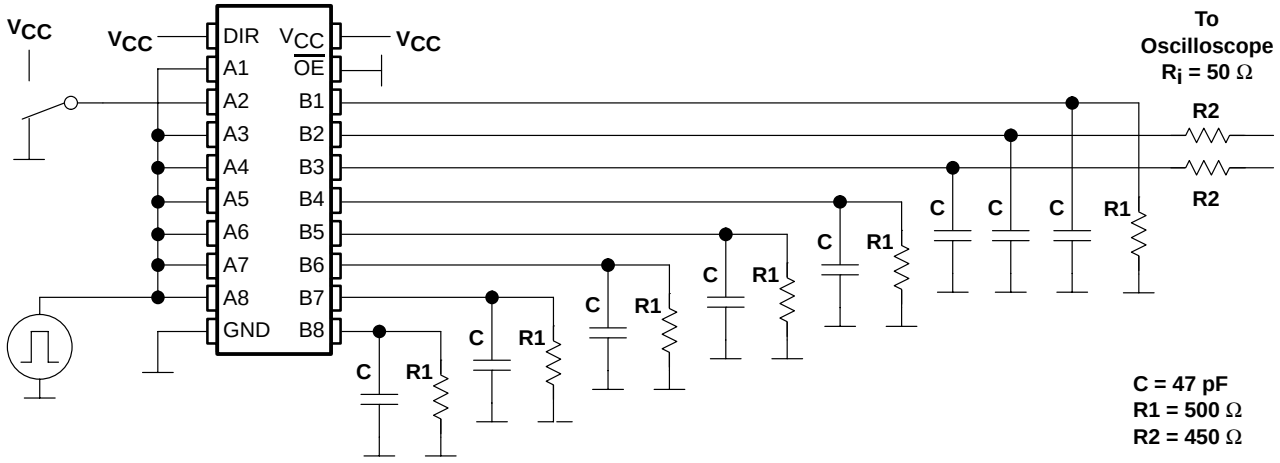


Figure 23. Circuit for Evaluating Simultaneous-Switching Noise (8-Bit SN74AHC245, V_{CC} = 5 V)

Figure 24 shows the interference voltage that arises when simultaneously switching several outputs as measured on an SN74AHC245 bus-interface device in a dual-in-line (N) package. The measured output B2 (see Figure 23) is at a low logic level, while seven other outputs are switched simultaneously from high to low.

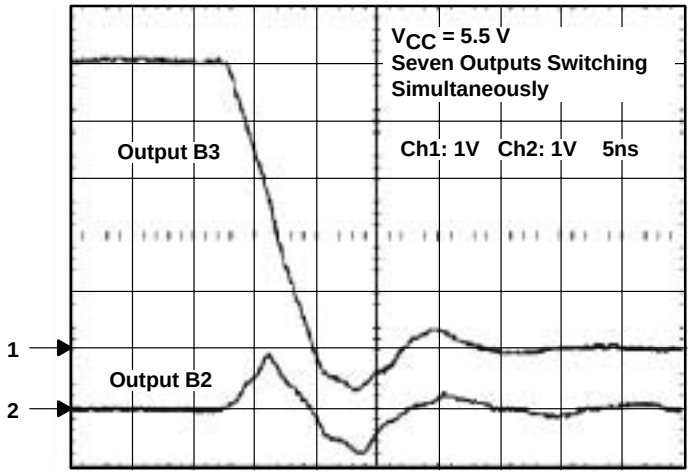


Figure 24. Simultaneous-Switching Noise of SN74AHC245 (V_{CC} = 5.5 V)

With a reduction of the supply voltage, the output current supplied by the circuit is also reduced. The simultaneous-switching noise (see Figure 25) also is reduced.

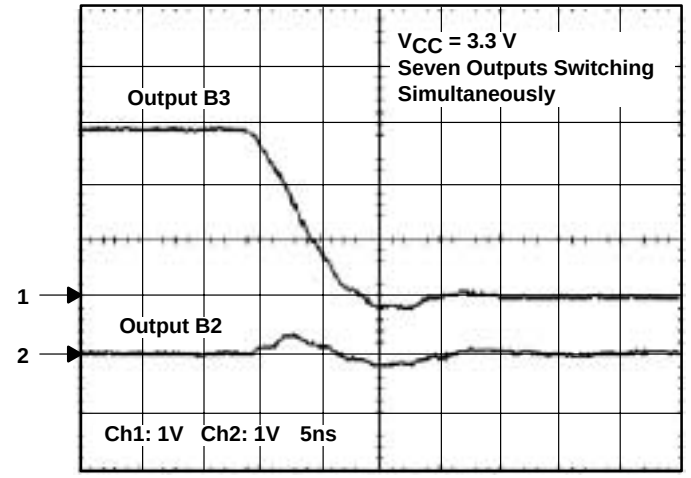


Figure 25. Simultaneous-Switching Noise of SN74AHC245 (V_{CC} = 3.3 V)

A general conclusion can be drawn from the considerations detailed previously that packages intended for surface mounting (for example, the SO package) should show significantly better behavior than packages that are considerably larger and are intended for through-hole mounting (DIL package), because their smaller mechanical dimensions should lead to lower values for the inductances of the internal connections. These conclusions are basically correct, as shown in Table 5. However, if the inductances of the supply pins of a circuit are reduced, the primary result will be an increase in speed because of improved voltage response, which is, for example, evidenced by a significantly shorter delay time. For this reason, the interference voltages measured on SO packages typically are only about 10% to 20% smaller than with DIL packages. Only when critical inductances are reduced to below about 2 nH will the interference become smaller in proportion to the reduction of the inductances. Below this value, experience has shown that the speed of the circuit is determined by the limits imposed by the semiconductor technology.

Table 5. Inductances of a 20-Pin Package

PACKAGE	PIN INDUCTANCE AT THE ENDS OF THE PACKAGE (PINS 1, 10, 11, 20)	PIN INDUCTANCE IN THE MIDDLE OF THE PACKAGE (PINS 5, 6, 15, 16)
DIL	13,7 nH	3,4 nH
SO	4,2 nH	2,4 nH

Besides the effect of the voltage drop across the inductances of the supply lines, the amplitude of the noise voltage also is determined by the cross talk between the pins of the package. One of the consequences is that the measured interference voltage is at a maximum at those pins that have simultaneously switching outputs on both sides. Conversely, interference voltages at the ends of the package are significantly lower. When low distortion of the signal is particularly important in specific applications, the latter situation can be attained by appropriate routing of the signals. As a result of the many supply voltage connections distributed around the perimeter of Widebus packages (see Figure 26), harmful inductance is reduced in accordance with the number of parallel electrical connections. Also, supply lines between the signal lines reduce the coupling between signal lines, further contributing to the low level of interference voltage.

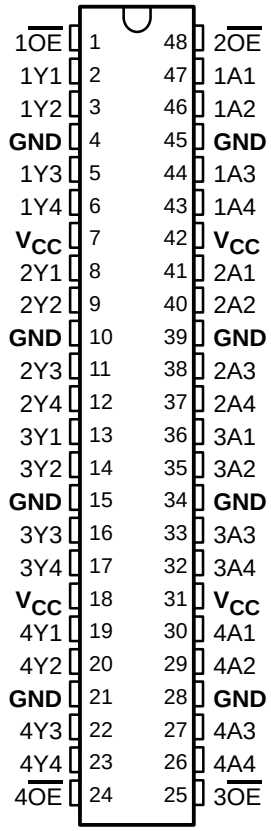


Figure 26. Pin Layout of an SN74AHC16244 Widebus Device

3.3 Signal Transmission

The principal purpose of digital devices (besides implementing logic functions) is driving other digital circuits. In some cases, the devices can be connected on a printed circuit board by printed wires that are only a few millimeters long or in other cases, a bus line connects several other transmitters and receivers (transceivers). The behavior of AHC circuits under a variety of operating conditions is discussed in the following paragraphs.

3.3.1 Point-to-Point Connections

For point-to-point connections (see Figure 27), line impedances of 70 Ω to 100 Ω for the conductors on circuit boards can be assumed. The line is terminated at its end by a circuit that essentially is as shown in Figure 27. For positive voltages, this line termination has a high resistance and negative-going overshoots are limited by clamping diode D1. Under these conditions, AHC circuits will have no problem driving the loads connected to them.

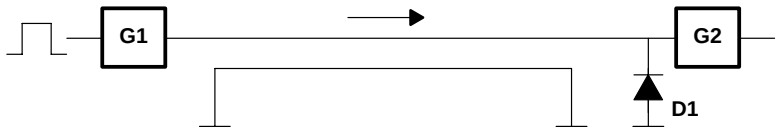


Figure 27. Typical Point-to-Point Connection

Figure 28 shows the waveform at the beginning and at the end of a line having an impedance, Z_O, of about 100 Ω. Because output impedance of the circuit is about 35 Ω, overshoots and undershoots at the end of the line are sufficiently limited. The clamping diode at the input of the receiver circuit limits negative voltages to acceptable values.

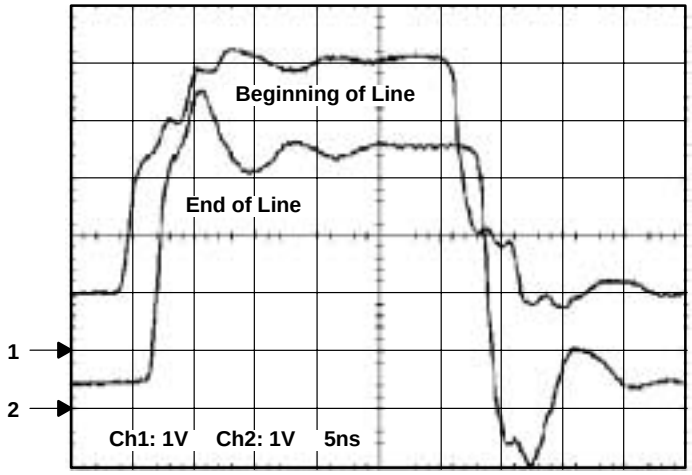


Figure 28. Waveform in a Point-to-Point Connection

In some cases it may be necessary to take additional precautions to reduce distortion resulting from reflections at the line ends. The options are to provide an appropriate termination at the end of the line or a matching circuit at the beginning of the line.

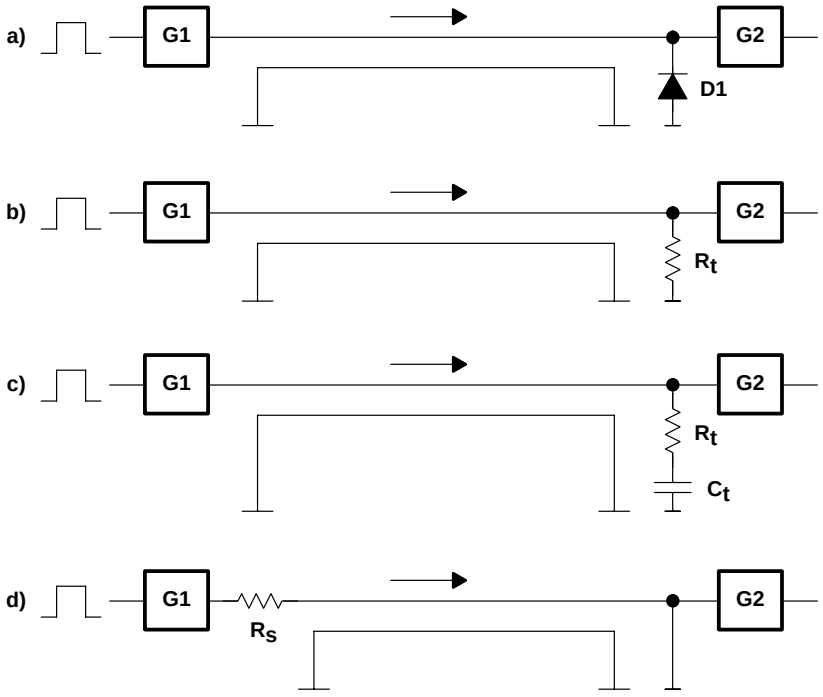


Figure 29. Line Termination and Matching

The use of clamping diodes (D1 in Figure 29a) is the most effective method of termination, especially when the protection diodes already incorporated in the input circuits of AHC devices can take on this job. In some cases, limiting positive overshoots may also be advisable. In this case, additional diodes should be connected between the input and the positive supply-voltage connection terminal.

The use of termination resistors of the proper value at the end of the line (R_t in Figure 29b) produce ideal waveforms. However, the higher power dissipation in the termination resistors, which results from this arrangement, usually outweighs the advantage of the low distortion of the signal.

If a termination at the end of the line cannot be avoided, connecting a termination resistor and a capacitor in series is recommended. This blocks dc from the terminating network and reduces power consumption of the circuit. Capacitor C_t in Figure 29c is chosen so that the time constant $R_t \times C_t$ is approximately four times the signal propagation time along the line.

A more elegant method of preventing undershoots and overshoots at the end of the line consists of matching the output impedance of the line driver with a series resistor (R_S in Figure 29d) to the line impedance. This makes optimum matching possible, without adversely affecting the balancing of the line.

3.3.2 Bus Lines

In addition to point-to-point connections previously mentioned, bus lines have great importance in computer systems. In this application several transmitter and receiver circuits, or combinations of them as transceivers, are situated along a line (see Figure 30). Each of these circuits loads the system with its input capacitance, which leads to a significantly longer signal propagation time ($t_p \approx 20$ ns/m) and to line impedances, Z_O, of about 30 Ω.

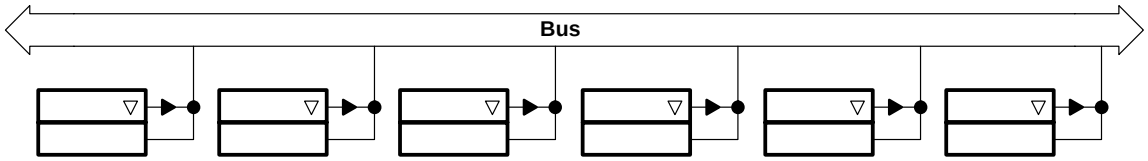


Figure 30. Bus Line

Because line impedances are now the same as, or smaller than, the output impedances of the AHC circuits, no more undershoots or overshoots occur at the end of the line (see Figure 31). Thus, in general, it is possible to dispense completely with line terminations. However, because of the unfavorable impedance relationships, four to six signal-propagation time periods will have passed before the desired logic level is reached. In smaller systems, and with bus lines having a length of only a few centimeters, this disadvantage is acceptable. The possibility of being able to dispense almost entirely with precautions to prevent reflections along the line usually completely outweighs the disadvantage of the longer settling time. With longer bus lines and their resultant longer settling times, voltage levels will exist for a longer time at the inputs of the receivers connected to the bus, which do not conform to the nominal voltage of the input signal. Figure 31 shows that with the incident wave at the end of the line, a level has been reached that is only very close to the threshold voltage of the receivers that are connected. In these circumstances, operation of the circuit without problems cannot be ensured. With longer bus lines and when shorter settling times are needed, components with better drive capability, such as those from the series SN74LVC and SN74ALVC, should be used.

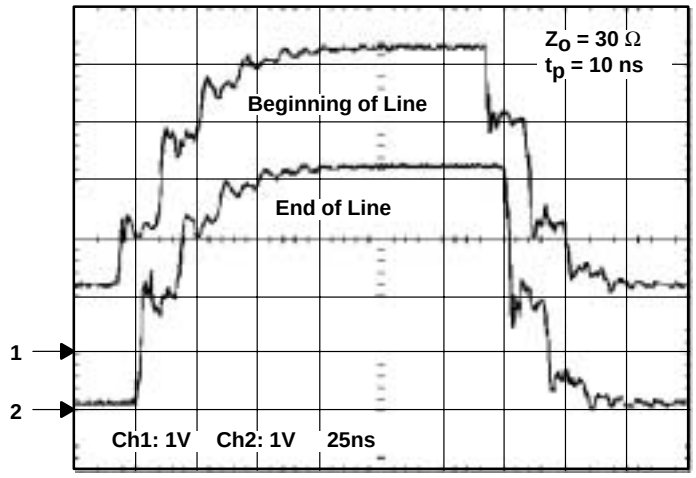


Figure 31. Waveform on a Bus Line

3.4 Behavior With Slow Signal Edges

During the development of the AHC devices, precautions were taken to prevent the internal circuit of the devices from oscillating with input signals having slow edges. The hysteresis built into the input stages provides for operation without problems only with signals that are usually delivered by logic circuits. The permissible transition time of the input signal is given in the data sheet as t_B = 10 ns/V. With a signal swing of 5 V, this corresponds to a rise and fall time $t_{r/t}$ < 45 ns. If a typical rise time of the output signals of AHC circuits of $t_{r/f}$ < 5 ns is assumed, there is a sufficient margin available within the circuit. In practice, input circuits also can typically process signals with significantly slower edges. Figure 32 shows the behavior of SN74AHC244 bus-interface device when it is controlled by extremely slow signals ($t_f \approx$ 100 ns). Even under these conditions, the device shows no tendency to oscillate. However, this example should not tempt the system designer generally to allow signals with such slow edges. If rise times of the input signal that lie outside the previously given specification can be expected, the Schmitt trigger, which has been specially developed for this application, always should be used.

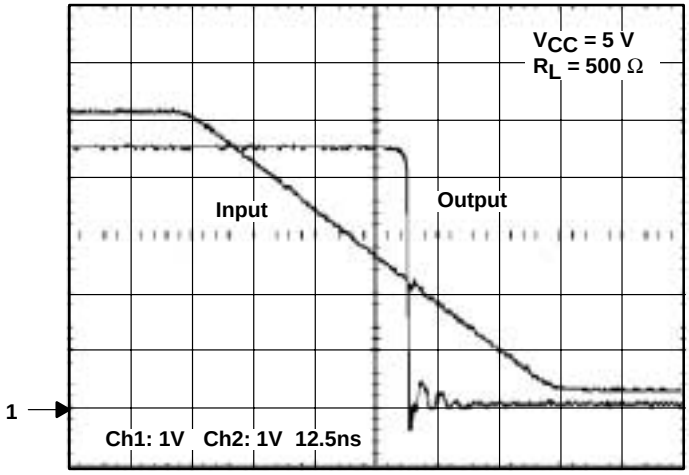


Figure 32. Behavior With Extremely Slow Input Signals

4. Special Application Problems

For several years, systems have been designed and manufactured to use two or more supply voltages, 3.3 V and 5 V. The reason is that, with the introduction of the so-called low-voltage logic circuits, all components needed were not available and, in some cases, still are not. Therefore, often there was no alternative but to use integrated circuits requiring a supply voltage of 5 V in systems conceived for a supply voltage of 3.3 V. Special circuit techniques are then required at the interfaces. The problems involving the use of several supply voltages can be expected to increase in the future. With components having structures of <0.5 µm being manufactured, still lower operating voltages will be needed, and the problem mentioned above will appear again in another form. Level conversion and matching will remain an applications problem.

4.1 Level Matching and Conversion

Level matching between parts of circuits that operate with different supply voltages, for example, 3.3 V and 5 V, is very simple if AHC and AHCT circuits are used (see Figure 33). Protection circuits at the inputs of these components do not contain any diodes between the input and the supply-voltage connection. The problem of feedback from a part of the circuit that is switched off does not exist.

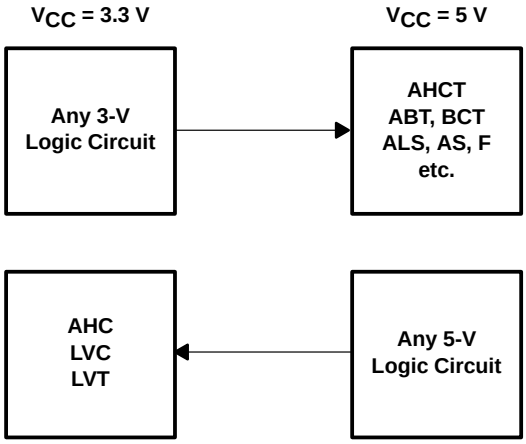


Figure 33. Level Conversion

All circuits designed for V_{CC} = 3.3 V deliver TTL-compatible signal levels at their outputs. When controlling parts of the circuit that operate at V_{CC} = 5 V, TTL-compatible devices must be used on the 5-V side. Also, these integrated circuits must not have any of the clamping diodes mentioned above. For this purpose, AHCT devices, as well as all bipolar and BiCMOS circuits are suitable. HCT and ACT devices should not be used. Level problems should not be expected when choosing suitable interface circuits for level converters from 5 V to 3 V. With few exceptions, for example, ALVC, devices that have been designed for V_{CC} = 3.3 V can be controlled with a signal swing of up to 5 V. Also, in this case, care must be taken that only components are used on the 3.3-V side that do not contain the clamping diodes mentioned above. Circuits from the series SN74HC, SN74AC, and SN74LV are not suitable for this purpose.

Table 6. Level Converters, 5 V to 3.3 V

FROM V_{CC} = 5 V	TO V_{CC} = 3 V							
	LV	LVC	ALVC	HC	AC	AHC	LVT	ALVT
Bipolar TTL	No	Yes	No	No	No	Yes	Yes	Yes
BiCMOS (ABT, BCT)	No	Yes	No	No	No	Yes	Yes	Yes
CMOS	No	Yes	No	No	No	Yes	Yes	Yes

Table 7. Level Converters, 3.3 V to 5 V

FROM V_{CC} = 3.3 V	TO V_{CC} = 5 V				
	BIPOLAR TTL	BiCMOS (ABT, BCT)	AHCT	HC	AC
Any circuit	Yes	Yes	Yes	No	No

4.2 Partial Switching Off of Parts of a System

Partial switching off of parts of a system occurs when part of an equipment or installation is switched off (without supply voltage) while other parts of the equipment remain in normal operation. This operating situation occurs regularly at the interfaces with other equipment. The same state can be observed frequently within a module that operates with several supply voltages, for example, 3.3 V and 5 V. Since the individual power supplies are not switched on and off simultaneously and in coordination, the case in which one or other power supply does not deliver the required voltage must be considered. The simplified output circuit of an AHC/AHCT device is shown in Figure 8. Diode D1 short circuits the output to ground when the supply voltage is switched off (V_{CC} = 0 V). Since this diode has a very low resistance (see Figure 11), this operating state is a defined low-logic level. To this extent, such a circuit provides a defined level. This behavior has disadvantages in bus systems. If the supply voltage of one of the subscribers connected to the bus is switched off, its output short circuits the complete bus line. A solution in such a case can be provided only by using bipolar and BiCMOS circuits, which do not have the diodes shown in Figure 8 in their output stages. In this connection, special mention should be made of the circuits from the SN74ABT and SN74LVT series.

Many of the interface problems discussed here can be solved very easily using integrated circuits specially developed for this purpose, such as the bidirectional 8-bit Widebus transceiver SN74LVC4245 (see Figure 34), or its 16-bit Widebus version SN74ALVC164245. These components have two separate supply-voltage connections [V_{CCA} (5 V) and V_{CCB} (3.3 V)]. In this way it is possible to solve the problems previously discussed by means of appropriate circuitry within the component. The engineer developing a system will no longer be concerned with these problems.

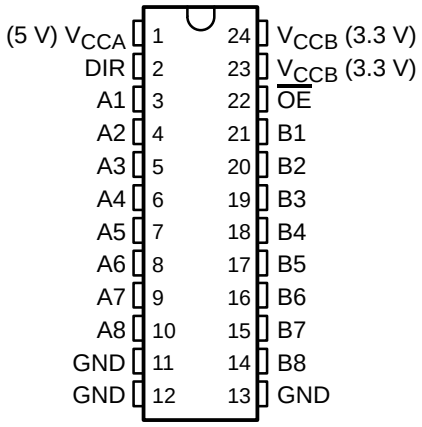


Figure 34. Pin Layout of SN74LVC4245 Transceiver

5. Comparison of AHC and HC Circuits

High-speed CMOS and advanced CMOS circuits have been used for more than a decade in many diverse applications. The HC circuits feature comparatively simple application rules, and this has encouraged their widespread use. AC circuits are found in applications in which high speed (i.e., short delay times) and high drive capability are required. The latter advantages must be weighed against the considerable internal noise (ground bounce, cross talk, etc.) that these circuits generate.

The ideal situation was a combination of the advantages of both logic families. Maintaining the moderate drive capability of HC circuits, which ensures a low internal-noise level, and incorporating the technical advantages offered by a modern manufacturing process with structures of 1 μm, the creation of the advanced high-speed CMOS family became a reality. In addition, particular attention was paid to the increasing trend toward applications operating with supply voltages of only 3.3 V. A number of improvements were also incorporated that facilitate applications with these components: changes to the input circuits, and improved ESD protection. The most important parameters are summarized in Table 8.

Table 8. Comparison of the Logic Families

	PRODUCT FAMILY				
	AHC		HC	LVC	AC
Technology	CMOS		CMOS	CMOS	CMOS
Structure (gate length)	1 μm		2–3 μm	0.8 μm	1 μm
5-V tolerant?	Yes		No	Yes	No
Gate and bus-interface circuits available?	Yes		Yes	Yes	Yes
Widebus circuits (16 bit) available?	Yes		No	Yes	Yes
Bus-hold circuit?	No		No	Yes	No
	V_{CC} = 5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	V_{CC} = 3.3 V	V_{CC} = 5 V
Supply current, I_{CC} ('245)	40 μA	40 μA	80 μA	10 μA	40 μA
Output current	–8/8 mA	–4/4 mA	–6/6 mA	–24/24 mA	–24/24 mA
Delay time, $t_{pd(max)}$ ('245)	6.5 ns	10 ns	26 ns	7.5 ns	9 ns
Input capacitance, C_i ('245)	2.5 pF		4.6 pF	3.3 pF	4.5 pF
Input/output capacitance, C_{io} ('245)	8 pF		16 pF	5.4 pF	15 pF

6. Package Construction

The trend toward further miniaturization of equipment and appliances is continuing, as indicated by the huge range of portable battery-operated equipment now available. Manufacturers of semiconductors are making a major contribution to this trend, because miniaturization can be realized only with smaller packages and corresponding progress in manufacturing technology. System designers always should remain aware of the problems involved in the use of modern packages.

Special manufacturing techniques when encapsulating the integrated circuits (chips) in their packages are employed to overcome problems that can occur. Everything possible must be done to eliminate humidity inside the package. This humidity has less to do with possible corrosion of the integrated circuits because, for the last 20 years, surfaces of all chips have been passivated with a glass layer (nitride), and possible corrosion has lost its significance. Any humidity trapped in the package shows up as a problem with the soldering techniques, for example, flow-soldering baths, now used for surface-mounted components. During the soldering process, humidity can vaporize and cause the package to burst (the “popcorn” effect). Immediately after manufacture, the devices must be stored in a special packing (Dry Pack) and, in some cases, in air-conditioned rooms.

The handling of ever-smaller packages presents a problem for the manufacturing engineer. With a pin spacing of only 0.4 mm, such as that attained with the thin shrink small-outline packages (TSSOP), exceptional demands are placed on soldering techniques, such as the accuracy with which the components are placed in assembly and the precise control of the soldering process. In the past, difficulty in controlling the soldering process often has been responsible for delaying the introduction of smaller packages.

Although maximum permissible power dissipation of the small packages is of secondary significance only for the AHC circuits, miniaturization of components obviously has reduced their ability dissipate heat. The relationships are explained in Table 9. With AHC circuits in the middle-speed class, thermal impedance usually is of little importance; these devices have an extremely low quiescent current drain. Also, in the frequency range up to about 10 MHz, in which these components should be used, the dynamic power dissipation is kept within reasonable limits. In individual cases, for example, at high clock frequencies or with the use of Widebus circuits, the system designer should calculate the power dissipation that can be expected to prevent overloading of these components.

Table 9. Thermal Impedance of 20-Pin Packages

PARAMETER	PACKAGE					UNIT
	DIL	SOP	SSOP	TSSOP	TVSOP	
Thermal impedance, θ_{JA}	67	96.6	104.2	148.9	179.5	°C/W

Figure 35 provides mechanical dimensions of the various packages in which AHC/AHCT families are available. This table is not all inclusive because the many variants of different numbers of package pins from 14 to 56 cannot be shown in the space available. The spectrum of available packages extends from the very well-known and much-used dual-in-line package (DIL), through the well-established small outline package (SO) and up to the thin very small-outline package (TVSOP). With a pin spacing of only 0.4 mm (16 mil) and a height of 1.2 mm, this package is ideal for use in chip cards.

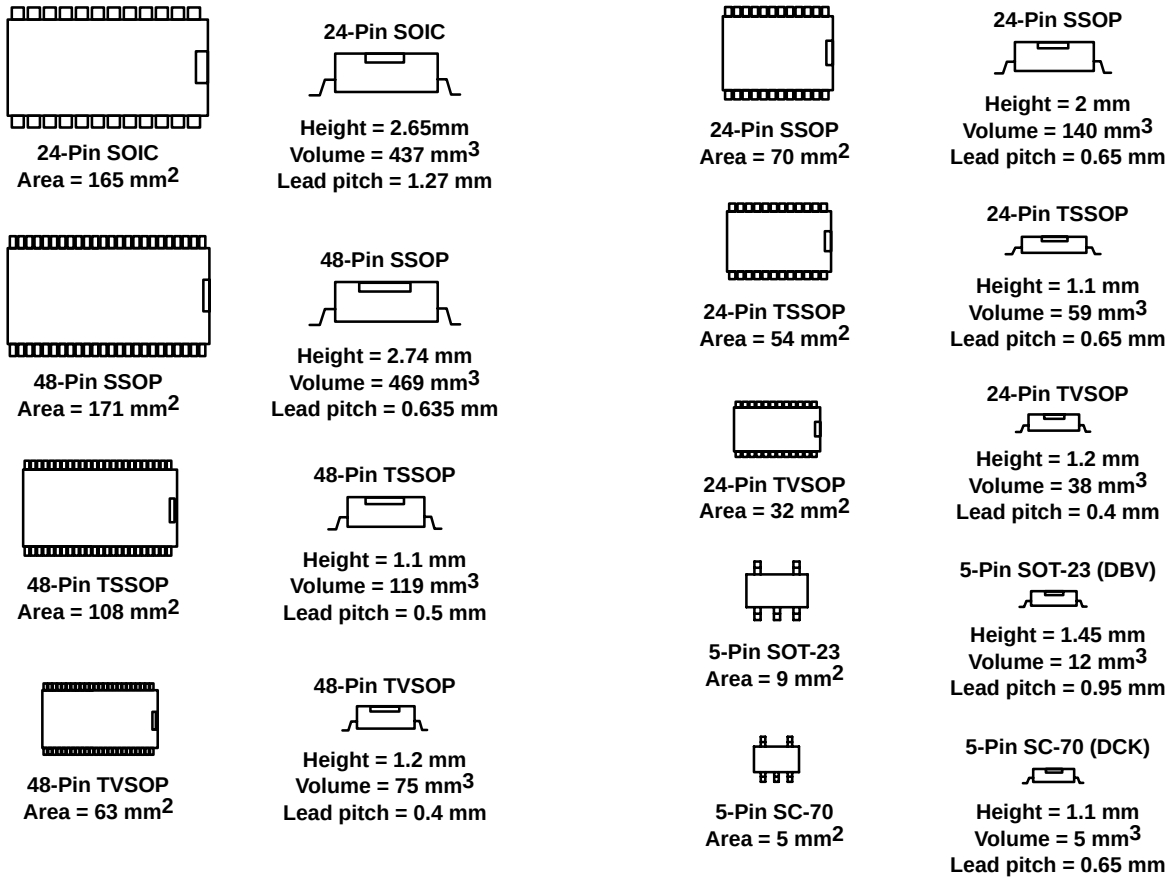


Figure 35. Selected Package Dimensions

6.1 Single-gate Logic

System designers often are confronted with the need for another gate or inverter to complete the design. The reason for this additional component may be, for example, that a signal from one circuit can supply the logic level needed by the subsequent circuit only after inversion. Or, at the last moment, it may be realized that the logical combination of two signals (AND, OR) is needed to implement the required function. Finally, it can be determined that the input signal needs to be amplified or that a Schmitt trigger is required to make an edge steeper so that a following circuit will operate properly.

In the past when this situation arose, it was necessary to incorporate an additional 14- or 16-pin package, which might have been only 25% utilized. Besides the cost of this additional component, the space required becomes of great importance when equipment and systems need to be miniaturized. To meet this need, the Microgate Logic and Picogate Logic packages have been developed. The Microgate Logic circuits are supplied in a 5-pin SOT-23 package, and the Picogate Logic circuits in the still smaller SC-70 package (Figure 35). The dimensions of Microgate Logic conform to those of the SOT-23, which has long been used for small-signal transistors and has been extended with two additional pins. It should be emphasized that the 5-pin SOT-23 package originally was introduced for use with analog circuits. In analog circuit practice there are far fewer opportunities to construct circuits (such as amplifiers) with standardized components than is the case in digital circuitry where all circuits are basically derived from gates or inverters. Because amplifiers or comparators are chosen for specific functions in the application, the SOT-23 package containing the required function is the logical choice.

Because the SOT-23 package has only five pins, of which two need to be reserved for the supply voltage, the functions that can be integrated into them are limited: AND, NAND, OR, NOR, EXOR gates, and inverters. Other functions, such as the Schmitt trigger, are available that are particularly needed in interfaces. An available often-used function is the unbuffered inverter, designated as ’04U (U = unbuffered). This device has applications in oscillators, and can be used as an analog wideband amplifier.

7. Summary

With their advanced high-speed CMOS logic family, TI has created a series of components that combines the advantages of many integrated circuits that are already well known, without having to accept many of their disadvantages:

- All CMOS circuits have low power requirements in common.
- Delay times have been much improved in comparison with HC devices.
- Values have been reached that were previously possible only with AC devices.

The high driveability of the latter family has not been incorporated – this is reserved for the AC, LVC, and ALVC families – but instead they have been limited in this respect to values that are usual for high-speed CMOS. From the point of view of interference that integrated circuits themselves generate, these components are easy to use. This ease of use extends from their dynamic-power dissipation and low cross talk between signal lines to the precautions necessary to ensure the electromagnetic compatibility of a circuit or system.

8. References

1. Texas Instruments, *AHC/AHCT, HC/HCT, and LV CMOS Logic Data Book*, literature number SCLD004.
2. Texas Instruments, *Semiconductor Group Package Outlines Reference Guide*, literature number SSYU001.
3. *Fachverband Bauelemente der Elektronik: Messung der EME von integrierten Schaltungen* (Professional Association for Electronic Components: Measuring the EME of Integrated Circuits).
4. Texas Instruments, *Digital Design Seminar,* literature number SDYDE01A.

Appendix A

Product Portfolio

ADDITIONAL LITERATURE

For more information on the AHC product line, please visit:

http://www.ti.com/sc/ahc
http://www.ti.com/sc/littlelogic

If you would like additional AHC literature, please call 1-800-477-8924 and ask for the following items:

TITLE	LITERATURE NUMBER
Logic Selection Guide and Data Book CD-ROM	SCBC001
Logic Selection Guide	SDYU001
Logic Solutions Overview Brochure (1998)	SCAB003
AHC/AHCT Logic Advanced High-Speed CMOS Data Book	SCLD003
Design Considerations for Logic Products Application Book (1997)	SDYA002
Design Considerations for Logic Products Application Book Volume 2 (1999)	SDYA018

PRODUCT AVAILABILITY

Refer to the following codes for column entries on the following pages.

military package description and availability

CDIP (ceramic dual-in-line package)
J = 14/16/20 pins
JT = 24/28 pins

CFP (ceramic flat package)
WA = 14 pins (small outline)
W = 14/16/20 pins
WD = 48/56 pins

CPGA (ceramic pin grid array)
GB = 68/84/120 pins

CQFP (ceramic quad flat package)
HV = 68 pins
HT = 84 pins
HS = 100 pins
HFP = 132 pins

LCCC (leadless ceramic chip carrier)
FK = 20/28 pins

schedule

✔ = Now
✣ = Planned
★ = Please see the corresponding device data sheet for correct military nomenclature or visit http://www.ti.com/sc/docs/military for TI military product information.

APPENDIX A
PRODUCT AVAILABILITY
AHC

DEVICE	NO. PINS	DESCRIPTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SOT	SSOP	TSSOP	TVSOP	
SN74AHC00	14	Quad 2-Input NAND Gates	✔	✔	✔		✔	✔	✔	SCLS227E
SN74AHC02	14	Quad 2-Input NOR Gates	✔	✔	✔		✔	✔	✔	SCLS254G
SN74AHC04	14	Hex Inverters	✔	✔	✔		✔	✔	✔	SCLS231I
SN74AHCU04	14	Unbuffered Hex Inverters	✔	✔	✔		✔	✔	✔	SCLS234G
SN74AHC05	14	Hex Inverters with Open-Drain Outputs		✔	✔		✔	✔	✔	SCLS357E
SN74AHC08	14	Quad 2-Input AND Gates	✔	✔	✔		✔	✔	✔	SCLS236D
SN74AHC14	14	Hex Schmitt-Trigger Inverters	✔	✔	✔		✔	✔	✔	SCLS238E
SN74AHC32	14	Quad 2-Input OR Gates	✔	✔	✔		✔	✔	✔	SCLS247D
SN74AHC74	14	Dual D-Type Flip-Flops with Set and Reset	✔	✔	✔		✔	✔	✔	SCLS255F
SN74AHC86	14	Quad 2-Input Exclusive-OR Gates	✔	✔	✔		✔	✔	✔	SCLS249E
SN74AHC123A	16	Dual Retriggerable Monostable Multivibrators with Reset	✔	✔	✔		✔	✔	✔	SCLS352D
SN74AHC125	14	Quad Bus Buffers with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS256F
SN74AHC126	14	Quad Bus Buffers with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS257I
SN74AHC132	14	Quad 2-Input NAND Gates with Schmitt-Trigger Inputs		✔	✔		✔	✔	✔	SCLS365D
SN74AHC138	16	3-to-8 Line Inverting Decoders/Demultiplexers	✔	✔	✔		✔	✔	✔	SCLS258H
SN74AHC139	16	Dual 2-to-4 Line Decoders/Demultiplexers		✔	✔		✔	✔	✔	SCLS259G
SN74AHC157	16	Quad 2-to-4 Line Data Selectors/Multiplexers	✔	✔	✔		✔	✔	✔	SCLS345E
SN74AHC158	16	Quad 2-to-4 Line Data Selectors/Multiplexers		✔	✔		✔	✔	✔	SCLS346D
SN74AHC240	20	Octal Buffers/Drivers with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS251E
SN74AHC244	20	Octal Buffers and Line Drivers with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS226G
SN74AHC245	20	Octal Bus Transceivers with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS230F
SN74AHC273	20	Octal D-Type Flip-Flops with Clear	✔	✔	✔		✔	✔	✔	SCLS376D
SN74AHC367	16	Hex Buffer/Line Drivers with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS424C
SN74AHC373	20	Octal Transparent D-Type Latches with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS235F
SN74AHC374	20	Octal D-Type Edge-Triggered Flip-Flops with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS240F
SN74AHC540	20	Inverting Octal Buffers and Line Drivers with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS260G
SN74AHC541	20	Octal Buffers and Line Drivers with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS261J
SN74AHC573	20	Octal Transparent D-Type Latches with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS242H
SN74AHC574	20	Octal Edge-Triggered D-Type Flip-Flops with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS244F
SN74AHC594	16	8-Bit Shift Registers with Output Registers		✔	✔		✔	✔		SCLS423B
SN74AHC595	16	8-Bit Shift Registers with 3-State Output Registers		✔	✔		✔	✔	✔	SCLS373D
SN74AHC16240	48	16-Bit Buffers/Drivers with 3-State Outputs					✔	✔	✔	SCLS326F
SN74AHC16244	48	16-Bit Buffers/Drivers with 3-State Outputs					✔	✔	✔	SCLS327F
SN74AHC16373	48	16-Bit Transparent D-Type Latches with 3-State Outputs					✔	✔	✔	SCLS329F

commercial package description and availability

LFBGA (low-profile fine-pitch ball grid array)
GKE = 96 pins
GKF = 114 pins

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/68/84 pins

QFP (quad flatpack)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

TQFP (plastic thin quad flatpack)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

SOP (small-outline package)
PS = 8 pins
NS = 14/16/20/24 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

schedule

✔ = Now
✣ = Planned

DEVICE	NO. PINS	DESCRIPTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SOT	SSOP	TSSOP	TVSOP	
SN74AHC16374	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs					✔	✔	✔	SCLS330F
SN74AHC16540	48	16-Bit Buffers/Drivers with 3-State Outputs					✔	✔	✔	SCLS331E
SN74AHC16541	48	16-Bit Buffers/Drivers with 3-State Outputs					✔	✔	✔	SCLS332E
SN74AHC1G00	5	Single 2-Input NAND Gates				✔				SCLS313F
SN74AHC1G02	5	Single 2-Input NOR Gates				✔				SCLS342E
SN74AHC1G04	5	Single Inverters				✔				SCLS318H
SN74AHC1GU04	5	Single Inverters				✔				SCLS343I
SN74AHC1G08	5	Single 2-Input AND Gates				✔				SCLS314F
SN74AHC1G125	5	Single Bus Buffers with 3-State Outputs				✔				SCLS377D
SN74AHC1G126	5	Single Bus Buffers with 3-State Outputs				✔				SCLS379C
SN74AHC1G14	5	Single Schmitt-Trigger Inverters				✔				SCLS321G
SN74AHC1G32	5	Single 2-Input OR Gates				✔				SCLS317G
SN74AHC1G86	5	Single 2-Input Exclusive-OR Gates				✔				SCLS323F

APPENDIX A
PRODUCT AVAILABILITY
AHCT

DEVICE	NO. PINS	DESCRIPTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SOT	SSOP	TSSOP	TVSOP	
SN74AHCT00	14	Quad 2-Input NAND Gates	✔	✔	✔		✔	✔	✔	SCLS229G
SN74AHCT02	14	Quad 2-Input NOR Gates	✔	✔	✔		✔	✔	✔	SCLS262H
SN74AHCT04	14	Hex Inverters	✔	✔	✔		✔	✔	✔	SCLS232J
SN74AHCT08	14	Quad 2-Input AND Gates	✔	✔	✔		✔	✔	✔	SCLS237H
SN74AHCT14	14	Hex Schmitt-Trigger Inverters	✔	✔	✔		✔	✔	✔	SCLS246L
SN74AHCT32	14	Quad 2-Input OR Gates	✔	✔	✔		✔	✔	✔	SCLS248H
SN74AHCT74	14	Dual D-Type Flip-Flops with Set and Reset	✔	✔	✔		✔	✔	✔	SCLS263J
SN74AHCT86	14	Quad 2-Input Exclusive-OR Gates	✔	✔	✔		✔	✔	✔	SCLS250I
SN74AHCT123A	16	Dual Retriggerable Monostable Multivibrators with Reset	✔	✔	✔		✔	✔	✔	SCLS420C
SN74AHCT125	14	Quad Bus Buffers with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS264K
SN74AHCT126	14	Quad Bus Buffers with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS265L
SN74AHCT132	14	Quad 2-Input NAND Gates with Schmitt-Trigger Inputs		✔	✔		✔	✔	✔	SCLS366E
SN74AHCT138	16	3-to-8 Line Inverting Decoders/Demultiplexers	✔	✔	✔		✔	✔	✔	SCLS266I
SN74AHCT139	16	Dual 2-to-4 Line Decoders/Demultiplexers	✔	✔	✔		✔	✔	✔	SCLS267J
SN74AHCT157	16	Quad 2-to-4 Line Data Selectors/Multiplexers		✔	✔		✔	✔	✔	SCLS347H
SN74AHCT158	16	Quad 2-to-4 Line Data Selectors/Multiplexers		✔	✔		✔	✔	✔	SCLS348G
SN74AHCT240	20	Octal Buffers/Drivers with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS252H
SN74AHCT244	20	Octal Buffers and Line Drivers with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS228I
SN74AHCT245	20	Octal Bus Transceivers with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS233H
SN74AHCT273	20	Octal D-Type Flip-Flops with Clear		✔	✔		✔	✔	✔	SCLS375C
SN74AHCT367	16	Hex Buffers/Line Drivers with 3-State Outputs		✔	✔		✔	✔	✔	SCLS418C
SN74AHCT373	20	Octal Transparent D-Type Latches with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS239J
SN74AHCT374	20	Octal D-Type Edge-Triggered Flip-Flops with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS241I
SN74AHCT540	20	Inverting Octal Buffers and Line Drivers with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS268I
SN74AHCT541	20	Octal Buffers and Line Drivers with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS269L
SN74AHCT573	20	Octal Transparent D-Type Latches with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS243K
SN74AHCT574	20	Octal Edge-Triggered D-Type Flip-Flops with 3-State Outputs	✔	✔	✔		✔	✔	✔	SCLS245I
SN74AHCT594	16	8-Bit Shift Registers with Output Registers		✔	✔		✔	✔		SCLS417B
SN74AHCT595	16	8-Bit Shift Registers with 3-State Output Registers		✔	✔		✔	✔		SCLS374E
SN74AHCT16240	48	16-Bit Buffers/Drivers with 3-State Outputs					✔	✔	✔	SCLS333H
SN74AHCT16244	48	16-Bit Buffers/Drivers with 3-State Outputs					✔	✔	✔	SCLS334H
SN74AHCT16245	48	16-Bit Bus Transceivers with 3-State Outputs					✔	✔	✔	SCLS335H
SN74AHCT16373	48	16-Bit Transparent D-Type Latches with 3-State Outputs					✔	✔	✔	SCLS336G
SN74AHCT16374	48	16-Bit Edge-Triggered D-Type Flip-Flops with 3-State Outputs					✔	✔	✔	SCLS337G

commercial package description and availability

LFBGA (low-profile fine-pitch ball grid array)
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SOT (small-outline transistor)
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DCK = 5 pins

schedule

✔ = Now
✣ = Planned

DEVICE	NO. PINS	DESCRIPTION	AVAILABILITY							LITERATURE REFERENCE
			MIL	PDIP	SOIC	SOT	SSOP	TSSOP	TVSOP	
SN74AHCT16540	48	16-Bit Buffers/Drivers with 3-State Outputs					✔	✔	✔	SCLS338G
SN74AHCT16541	48	16-Bit Buffers/Drivers with 3-State Outputs					✔	✔	✔	SCLS339G
SN74AHCT1G00	5	Single 2-Input NAND Gates				✔				SCLS316H
SN74AHCT1G02	5	Single 2-Input NOR Gates				✔				SCLS341G
SN74AHCT1G04	5	Single Inverters				✔				SCLS319I
SN74AHCT1G08	5	Single 2-Input AND Gates				✔				SCLS315H
SN74AHCT1G14	5	Single Schmitt-Trigger Inverters				✔				SCLS322J
SN74AHCT1G32	5	Single 2-Input OR Gates				✔				SCLS320H
SN74AHCT1G86	5	Single 2-Input Exclusive-OR Gates				✔				SCLS324H
SN74AHCT1G125	5	Single Bus Buffers with 3-State Outputs				✔				SCLS378E
SN74AHCT1G126	5	Single Bus Buffers with 3-State Outputs				✔				SCLS380E