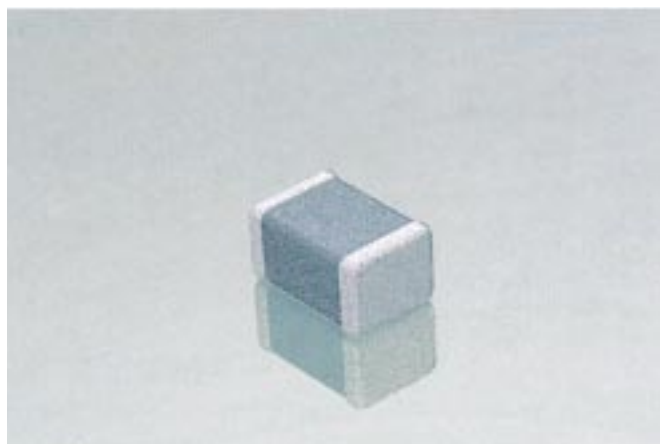


# C0G (NP0) Dielectric



## General Specifications



C0G (NP0) is the most popular formulation of the “temperature-compensating,” EIA Class I ceramic materials. Modern C0G (NP0) formulations contain neodymium, samarium and other rare earth oxides.

C0G (NP0) ceramics offer one of the most stable capacitor dielectrics available. Capacitance change with temperature is  $0 \pm 30 \text{ ppm}/^\circ\text{C}$  which is less than  $\pm 0.3\% \Delta C$  from  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ . Capacitance drift or hysteresis for C0G (NP0) ceramics is negligible at less than  $\pm 0.05\%$  versus up to  $\pm 2\%$  for films. Typical capacitance change with life is less than  $\pm 0.1\%$  for C0G (NP0), one-fifth that shown by most other dielectrics. C0G (NP0) formulations show no aging characteristics.

The C0G (NP0) formulation usually has a “Q” in excess of 1000 and shows little capacitance or “Q” changes with frequency. Their dielectric absorption is typically less than 0.6% which is similar to mica and most films.

## PART NUMBER (see page 3 for complete part number explanation)

**0805**

**Size**  
(L" x W")

**5**

**Voltage**  
25V = 3  
50V = 5  
100V = 1  
200V = 2

**A**

**Dielectric**  
C0G (NP0) = A

**101**

**Capacitance Code**

**J**

**Capacitance Tolerance**  
Preferred  
K =  $\pm 10\%$   
J =  $\pm 5\%$

**A**

**Failure Rate**  
A = Not Applicable

**T**

**Terminations**  
T = Plated Ni and Solder

**2**

**Packaging**  
2 = 7" Reel  
4 = 13" Reel

**A**

**Special Code**  
A = Std. Product

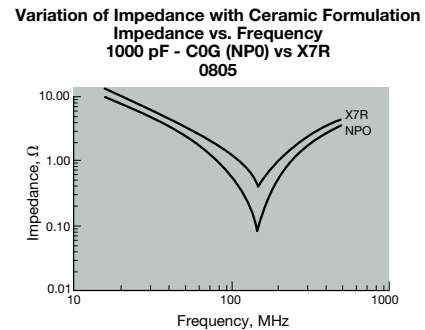
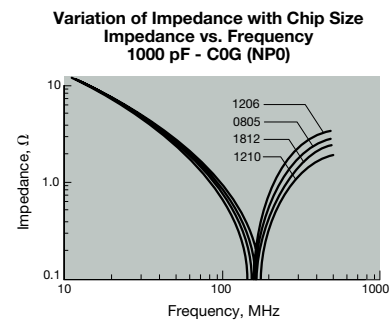
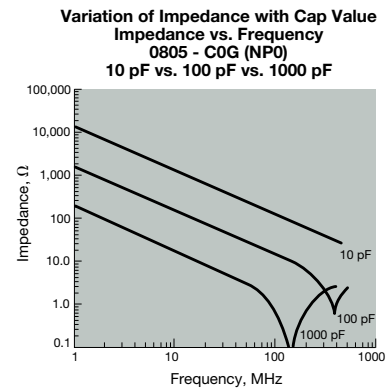
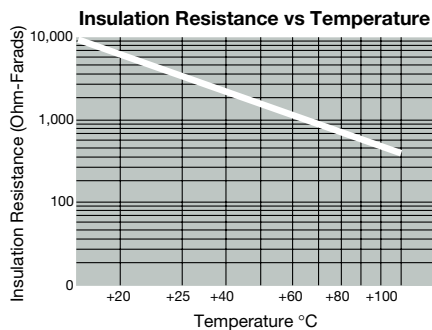
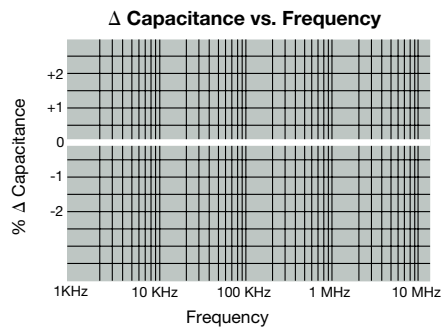
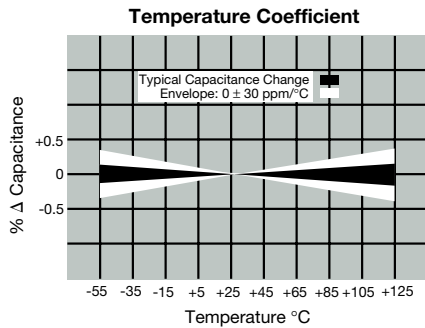
## PERFORMANCE CHARACTERISTICS

<b>Capacitance Range</b>	0.5 pF to .1 $\mu\text{F}$ (1.0 $\pm 0.2$ Vrms, 1kHz, for $\leq 100$ pF use 1 MHz)
<b>Capacitance Tolerances</b>	Preferred $\pm 5\%$ , $\pm 10\%$ others available: $\pm .25$ pF, $\pm .5$ pF, $\pm 1\%$ ( $\geq 25$ pF), $\pm 2\%$ ( $\geq 13$ pF), $\pm 20\%$ For values $\leq 10$ pF preferred tolerance is $\pm .5$ pF, also available $\pm .25$ pF.
<b>Operating Temperature Range</b>	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
<b>Temperature Characteristic</b>	$0 \pm 30$ ppm/ $^\circ\text{C}$ (EIA C0G)
<b>Voltage Ratings</b>	25, 50, 100 & 200 VDC ( $+125^\circ\text{C}$ )
<b>Dissipation Factor and “Q”</b>	For values $> 30$ pF: 0.1% max. ( $+25^\circ\text{C}$ and $+125^\circ\text{C}$ ) For values $\leq 30$ pF: “Q” = $400 + 20 \times C$ (C in pF)
<b>Insulation Resistance</b> ( $+25^\circ\text{C}$ , RVDC)	100,000 megohms min. or $1000 \text{ M}\Omega \cdot \mu\text{F}$ min., whichever is less
<b>Insulation Resistance</b> ( $+125^\circ\text{C}$ , RVDC)	10,000 megohms min. or $100 \text{ M}\Omega \cdot \mu\text{F}$ min., whichever is less
<b>Dielectric Strength</b>	250% of rated voltage for 5 seconds at 50 mamp max. current
<b>Test Voltage</b>	$1 \pm 0.2$ Vrms
<b>Test Frequency</b>	For values $\leq 100$ pF: 1 MHz For values $> 100$ pF: 1 KHz

# C0G (NP0) Dielectric



## Typical Characteristic Curves\*\*



## SUMMARY OF CAPACITANCE RANGES VS. CHIP SIZE

Style	25V	50V	100V	200V
0402*	0.5pF - 220pF	0.5pF - 120pF	—	—
0504	0.5pF - 330pF	0.5pF - 150pF	0.5pF - 68pF	—
0603*	0.5pF - 1nF	0.5pF - 1nF	0.5pF - 330pF	—
0805*	0.5pF - 4.7nF	0.5pF - 2.2nF	0.5pF - 1nF	0.5pF - 470pF
1206*	0.5pF - 10nF	0.5pF - 4.7nF	0.5pF - 2.2nF	0.5pF - 1nF
1210*	560pF - 10nF	560pF - 10nF	560pF - 3.9nF	560pF - 1.5nF
1505	—	10pF - 1.5nF	10pF - 820pF	10pF - 560pF
1808	→	1nF - 4.7nF	1nF - 3.9nF	1nF - 2.2nF
1812*	1nF - 15nF	1nF - 10nF	1nF - 4.7nF	1nF - 3.3nF
1825*	→	1nF - 22nF	1nF - 12nF	1nF - 6.8nF
2220	→	4.7nF - 47nF	4.7nF - 39nF	3.3nF - 27nF
2225	→	1nF - 100nF	1nF - 39nF	1nF - 39nF

\* Standard Sizes

\*\* For additional information on performance changes with operating conditions consult AVX's software SpiCap.



## Capacitance Range



**PREFERRED SIZES ARE SHADED**

SIZE		0402*			0504*			0603*			0805				1206				1505		
Standard Reel Packaging		All Paper			All Embossed			All Paper			Paper/Embossed				Paper/Embossed				All Embossed		
(L) Length	MM (in.)	1.00 ± .10 (.040 ± .004)			1.27 ± .25 (.050 ± .010)			1.60 ± .15 (.063 ± .006)			2.01 ± .20 (.079 ± .008)				3.20 ± .20 (.126 ± .008)				3.81 ± .25 (.150 ± .010)		
(W) Width	MM (in.)	.50 ± .10 (.020 ± .004)			1.02 ± .25 (.040 ± .010)			.81 ± .15 (.032 ± .006)			1.25 ± .20 (.049 ± .008)				1.60 ± .20 (.063 ± .008)				1.27 ± .25 (.050 ± .010)		
(T) Max. Thickness	MM (in.)	.60 (.024)			1.02 (.040)			.90 (.035)			1.30 (.051)				1.50 (.059)				1.27 (.050)		
(t) Terminal	MM (in.)	.25 ± .15 (.010 ± .006)			.38 ± .13 (.015 ± .005)			.35 ± .15 (.014 ± .006)			.50 ± .25 (.020 ± .010)				.50 ± .25 (.020 ± .010)				.50 ± .25 (.020 ± .010)		
WVDC		25	50		25	50	100	25	50	100	25	50	100	200	25	50	100	200	50	100	200
Cap (pF)	0.5 1.0 1.2 1.5																				
	1.8 2.2 2.7																				
	3.3 3.9 4.7																				
	5.6 6.8 8.2																				
	10 12 15																				
	18 22 27																				
	33 39 47																				
	56 68 82																				
	100 120 150																				
	180 220 270																				
	330 390 470																				
	560 680 820																				
	1000 1200 1500																				
	1800 2200 2700																				
	3300 3900 4700																				
	5600 6800 8200																				
	10000																				

**\*Reflow soldering only.**

NOTES: For higher voltage chips, see pages 20 and 21.

 = Paper Tape

 = Embossed Tape

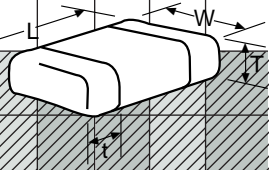
# C0G (NP0) Dielectric

## Capacitance Range



### PREFERRED SIZES ARE SHADED

SIZE		1210				1808*				1812*				1825*				2220*				2225*			
Standard Reel Packaging		Paper/Embossed				All Embossed				All Embossed				All Embossed				All Embossed				All Embossed			
(L) Length	MM (in.)	3.20 ± .20 (.126 ± .008)				4.57 ± .25 (.180 ± .010)				4.50 ± .30 (.177 ± .012)				4.50 ± .30 (.177 ± .012)				5.7 ± .40 (.225 ± .016)				5.72 ± .25 (.225 ± .010)			
(W) Width	MM (in.)	2.50 ± .20 (.098 ± .008)				2.03 ± .25 (.080 ± .010)				3.20 ± .20 (.126 ± .008)				6.40 ± .40 (.252 ± .016)				5.0 ± .40 (.197 ± .016)				6.35 ± .25 (.250 ± .010)			
(T) Max. Thickness	MM (in.)	1.70 (.067)				1.52 (.060)				1.70 (.067)				1.70 (.067)				2.30 (.090)				1.70 (.067)			
(t) Terminal	MM (in.)	.50 ± .25 (.020 ± .010)				.64 ± .39 (.025 ± .015)				.61 ± .36 (.024 ± .014)				.61 ± .36 (.024 ± .014)				.64 ± .39 (.025 ± .015)				.64 ± .39 (.025 ± .015)			
WVDC		25	50	100	200	50	100	200		25	50	100	200	50	100	200		50	100	200		50	100	200	
Cap (pF)	560																								
	680																								
	820																								
	1000																								
	1200																								
	1500																								
	1800																								
	2200																								
	2700																								
	3300																								
	3900																								
	4700																								
	5600																								
	6800																								
	8200																								
Cap. (μF)	.010																								
	.012																								
	.015																								
	.018																								
	.022																								
	.027																								
	.033																								
	.039																								
	.047																								
	.068																								
	.082																								
	.1																								



\*Reflow soldering only.

NOTES: For higher voltage chips, see pages 20 and 21.

= Paper Tape  
 = Embossed Tape

## I. Capacitance (farads)

English:  $C = \frac{.224 \text{ K A}}{T_D}$

Metric:  $C = \frac{.0884 \text{ K A}}{T_D}$

## II. Energy stored in capacitors (Joules, watt - sec)

$E = \frac{1}{2} CV^2$

## III. Linear charge of a capacitor (Amperes)

$I = C \frac{dV}{dt}$

## IV. Total Impedance of a capacitor (ohms)

$Z = \sqrt{R_s^2 + (X_C - X_L)^2}$

## V. Capacitive Reactance (ohms)

$X_C = \frac{1}{2 \pi fC}$

## VI. Inductive Reactance (ohms)

$X_L = 2 \pi fL$

## VII. Phase Angles:

Ideal Capacitors: Current leads voltage 90°

Ideal Inductors: Current lags voltage 90°

Ideal Resistors: Current in phase with voltage

## VIII. Dissipation Factor (%)

$D.F. = \tan \delta \text{ (loss angle)} = \frac{E.S.R.}{X_C} = (2 \pi fC) (E.S.R.)$

## IX. Power Factor (%)

P.F. = Sine  $\delta$  (loss angle) = Cos  $\phi$  (phase angle)

P.F. = (when less than 10%) = DF

## X. Quality Factor (dimensionless)

$Q = \cotan \delta \text{ (loss angle)} = \frac{1}{D.F.}$

## XI. Equivalent Series Resistance (ohms)

$E.S.R. = (D.F.) (X_C) = (D.F.) / (2 \pi fC)$

## XII. Power Loss (watts)

Power Loss =  $(2 \pi fCV^2) (D.F.)$

## XIII. KVA (Kilowatts)

$KVA = 2 \pi fCV^2 \times 10^{-3}$

## XIV. Temperature Characteristic (ppm/°C)

$T.C. = \frac{C_t - C_{25}}{C_{25} (T_t - 25)} \times 10^6$

## XV. Cap Drift (%)

$C.D. = \frac{C_1 - C_2}{C_1} \times 100$

## XVI. Reliability of Ceramic Capacitors

$\frac{L_o}{L_t} = \left( \frac{V_t}{V_o} \right)^X \left( \frac{T_t}{T_o} \right)^Y$

## XVII. Capacitors in Series (current the same)

Any Number:  $\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} \dots \frac{1}{C_N}$

Two:  $C_T = \frac{C_1 C_2}{C_1 + C_2}$

## XVIII. Capacitors in Parallel (voltage the same)

$C_T = C_1 + C_2 \dots + C_N$

## XIX. Aging Rate

$A.R. = \% \Delta C / \text{decade of time}$

## XX. Decibels

$db = 20 \log \frac{V_1}{V_2}$

## METRIC PREFIXES

## SYMBOLS

Pico	$\times 10^{-12}$	K	= Dielectric Constant	f	= frequency	$L_t$	= Test life
Nano	$\times 10^{-9}$	A	= Area	L	= Inductance	$V_t$	= Test voltage
Micro	$\times 10^{-6}$	$T_D$	= Dielectric thickness	$\delta$	= Loss angle	$V_o$	= Operating voltage
Milli	$\times 10^{-3}$	V	= Voltage	$\phi$	= Phase angle	$T_t$	= Test temperature
Deci	$\times 10^{-1}$	t	= time	X & Y	= exponent effect of voltage and temp.	$T_o$	= Operating temperature
Deca	$\times 10^{+1}$	$R_s$	= Series Resistance	$L_o$	= Operating life		
Kilo	$\times 10^{+3}$						
Mega	$\times 10^{+6}$						
Giga	$\times 10^{+9}$						
Tera	$\times 10^{+12}$						

# How to Order

## Part Number Explanation

### EXAMPLE: 08055A101JAT2A

<b>0805</b> Size (L" x W") <b>0402</b> 0504 <b>0603</b> <b>0805</b> 1005 0907 <b>1206</b> <b>1210</b> 1505 1805 1808 <b>1812</b> <b>1825</b> 2225 3640	<b>5</b>  <b>Voltage</b> 10V = Z 16V = Y 25V = 3 50V = 5 100V = 1 200V = 2 250V = V 500V = 7 600V = C 1000V = A 1500V = S 2000V = G 2500V = W 3000V = H 4000V = J 5000V = K	<b>A</b>  <b>Dielectric</b> COG (NP0) = A X7R = C X5R = D Z5U = E Y5V = G	<b>101</b>  <b>Capacitance Code</b> (2 significant digits + no. of zeros) Examples: 10 pF = 100 100 pF = 101 1,000 pF = 102 22,000 pF = 223 220,000 pF = 224 1 $\mu$ F = 105  For values below 10 pF, use "R" in place of decimal point, e.g., 9.1 pF = 9R1.	<b>J</b>  <b>Capacitance Tolerance</b> C = $\pm 0.25$ pF* D = $\pm 0.50$ pF* F = $\pm 1\%$ ( $\geq 25$ pF) G = $\pm 2\%$ ( $\geq 13$ pF) J = $\pm 5\%$ K = $\pm 10\%$ M = $\pm 20\%$ Z = $+80\%$ , $-20\%$ P = $+100\%$ , $-0\%$	<b>A</b>  <b>Failure Rate</b> A = Not Applicable	<b>T</b>  <b>Terminations</b> <b>Standard:</b> T = Ni and Tin Plated  Others: 7 = Plated Ni Gold Plated 1 = Pd/Ag	<b>2</b>  <b>Packaging**</b> <b>Recommended:</b> 2 = 7" Reel 4 = 13" Reel  Others: 7 = Bulk Cassette 9 = Bulk	<b>A</b>  <b>Special** Code</b> A = Standard Product  <b>Non-Standard</b> P = Embossed unmarked M = Embossed marked E = Standard packaging marked  <b>Low Profile Chips Only</b> Max. Thickness T = .66mm (.026") S = .56mm (.022") R = .46mm (.018")
---	---	--	--	---	---	---	--	---

\* C&D tolerances for  $\leq 10$  pF values.

\*\* Standard Tape and Reel material depends upon chip size and thickness.  
See individual part tables for tape material type for each capacitance value.

Note: Unmarked product is standard. Marked product is available on special request, please contact AVX.  
Standard packaging is shown in the individual tables.

Non-standard packaging is available on special request, please contact AVX.

## Environmental

### THERMAL SHOCK

#### Specification

##### Appearance

No visual defects

##### Capacitance Variation

C0G (NP0):  $\pm 2.5\%$  or  $\pm .25\text{pF}$ , whichever is greater  
 X7R:  $\leq \pm 7.5\%$   
 Z5U:  $\leq \pm 20\%$   
 Y5V:  $\leq \pm 20\%$

##### Q, Tan Delta

To meet initial requirement

##### Insulation Resistance

C0G (NP0), X7R: To meet initial requirement  
 Z5U, Y5V:  $\geq \text{Initial Value} \times 0.1$

##### Dielectric Strength

No problem observed

#### Measuring Conditions

Step	Temperature °C	Time (minutes)
1	C0G (NP0), X7R: $-55^\circ \pm 2^\circ$ Z5U: $+10^\circ \pm 2^\circ$ Y5V: $-30^\circ \pm 2^\circ$	$30 \pm 3$
2	Room Temperature	# 3
3	C0G (NP0), X7R: $+125^\circ \pm 2^\circ$ Z5U, Y5V: $+85^\circ \pm 2^\circ$	$30 \pm 3$
4	Room Temperature	# 3

Repeat for 5 cycles and measure after 48 hours  $\pm 4$  hours  
 (24 hours for C0G (NP0)) at room temperature.

### IMMERSION

#### Specification

##### Appearance

No visual defects

##### Capacitance Variation

C0G (NP0):  $\pm 2.5\%$  or  $\pm .25\text{pF}$ , whichever is greater  
 X7R:  $\leq \pm 7.5\%$   
 Z5U:  $\leq \pm 20\%$   
 Y5V:  $\leq \pm 20\%$

##### Q, Tan Delta

To meet initial requirement

##### Insulation Resistance

C0G (NP0), X7R: To meet initial requirement  
 Z5U, Y5V:  $\geq \text{Initial Value} \times 0.1$

##### Dielectric Strength

No problem observed

#### Measuring Conditions

Step	Temperature °C	Time (minutes)
1	+65 $\pm 5$ / $-0$ Pure Water	$15 \pm 2$
2	$0 \pm 3$ NaCl solution	$15 \pm 2$

Repeat cycle 2 times and wash with water and dry.  
 Store at room temperature for  $48 \pm 4$  hours (24 hours for C0G (NP0)) and measure.

### MOISTURE RESISTANCE

#### Specification

##### Appearance

No visual defects

##### Capacitance Variation

C0G (NP0):  $\pm 5\%$  or  $\pm .5\text{pF}$ , whichever is greater  
 X7R:  $\leq \pm 10\%$   
 Z5U:  $\leq \pm 30\%$   
 Y5V:  $\leq \pm 30\%$

##### Q, Tan Delta

C0G (NP0):  $\geq 30\text{pF}$  ..... Q  $\geq 350$   
 $\geq 10\text{pF}$ ,  $< 30\text{pF}$  ..... Q  $\geq 275+5C/2$   
 $< 10\text{pF}$  ..... Q  $\geq 200+10C$   
 X7R: Initial requirement + .5%  
 Z5U: Initial requirement + 1%  
 Y5V: Initial requirement + 2%

##### Insulation Resistance

$\geq \text{Initial Value} \times 0.3$

#### Measuring Conditions

Step	Temp. °C	Humidity %	Time (hrs)
1	+25- $\rightarrow$ +65	90-98	2.5
2	+65	90-98	3.0
3	+65- $\rightarrow$ +25	80-98	2.5
4	+25- $\rightarrow$ +65	90-98	2.5
5	+65	90-98	3.0
6	+65- $\rightarrow$ +25	80-98	2.5
7	+25	90-98	2.0
7a	-10	uncontrolled	—
7b	+25	90-98	—

Repeat 20 cycles (1-7) and store for 48 hours (24 hours for C0G (NP0)) at room temperature before measuring.  
 Steps 7a & 7b are done on any 5 out of first 9 cycles.

## Environmental

### STEADY STATE HUMIDITY

#### (No Load)

##### Specification

###### Appearance

No visual defects

###### Capacitance Variation

C0G (NP0):  $\pm 5\%$  or  $\pm .5\text{pF}$ , whichever is greater  
X7R:  $\leq \pm 10\%$   
Z5U:  $\leq \pm 30\%$   
Y5V:  $\leq \pm 30\%$

###### Q, Tan Delta

C0G (NP0):  $\geq 30\text{pF}$  ..... Q  $\geq 350$   
 $\geq 10\text{pF}$ ,  $< 30\text{pF}$  ..... Q  $\geq 275+5C/2$   
 $< 10\text{pF}$  ..... Q  $\geq 200+10C$   
X7R: Initial requirement + .5%  
Z5U: Initial requirement + 1%  
Y5V: Initial requirement + 2%

###### Insulation Resistance

$\geq$  Initial Value x 0.3

##### Measuring Conditions

Store at  $85 \pm 5\%$  relative humidity and  $85^\circ\text{C}$  for 1000 hours, without voltage. Remove from test chamber and stabilize at room temperature and humidity for  $48 \pm 4$  hours ( $24 \pm 2$  hours for C0G (NP0)) before measuring.

Charge and discharge currents must be less than 50ma.

##### Insulation Resistance

C0G (NP0), X7R: To meet initial value x 0.3  
Z5U, Y5V:  $\geq$  Initial Value x 0.1

Charge devices with rated voltage in test chamber set at  $85 \pm 5\%$  relative humidity and  $85^\circ\text{C}$  for 1000 (+48,-0) hours. Remove from test chamber and stabilize at room temperature and humidity for  $48 \pm 4$  hours ( $24 \pm 2$  hours for C0G (NP0)) before measuring.

Charge and discharge currents must be less than 50ma.

### LOAD LIFE

##### Specification

###### Appearance

No visual defects

###### Capacitance Variation

C0G (NP0):  $\pm 3\%$  or  $\pm .3\text{pF}$ , whichever is greater  
X7R:  $\leq \pm 10\%$   
Z5U:  $\leq \pm 30\%$   
Y5V:  $\leq \pm 30\%$

###### Q, Tan Delta

C0G (NP0):  $\geq 30\text{pF}$  ..... Q  $\geq 350$   
 $\geq 10\text{pF}$ ,  $< 30\text{pF}$  ..... Q  $\geq 275+5C/2$   
 $< 10\text{pF}$  ..... Q  $\geq 200+10C$   
X7R: Initial requirement + .5%  
Z5U: Initial requirement + 1%  
Y5V: Initial requirement + 2%

##### Insulation Resistance

C0G (NP0), X7R: To meet initial value x 0.3  
Z5U, Y5V:  $\geq$  Initial Value x 0.1

Charge devices with twice rated voltage in test chamber set at  $+125^\circ\text{C} \pm 2^\circ\text{C}$  for C0G (NP0) and X7R,  $+85^\circ \pm 2^\circ\text{C}$  for Z5U, and Y5V for 1000 (+48,-0) hours. Remove from test chamber and stabilize at room temperature for  $48 \pm 4$  hours ( $24 \pm 2$  hours for C0G (NP0)) before measuring.

Charge and discharge currents must be less than 50ma.

### LOAD HUMIDITY

##### Specification

###### Appearance

No visual defects

###### Capacitance Variation

C0G (NP0):  $\pm 5\%$  or  $\pm .5\text{pF}$ , whichever is greater  
X7R:  $\leq \pm 10\%$   
Z5U:  $\leq \pm 30\%$   
Y5V:  $\leq \pm 30\%$

###### Q, Tan Delta

C0G (NP0):  $\geq 30\text{pF}$  ..... Q  $\geq 350$   
 $\geq 10\text{pF}$ ,  $< 30\text{pF}$  ..... Q  $\geq 275+5C/2$   
 $< 10\text{pF}$  ..... Q  $\geq 200+10C$   
X7R: Initial requirement + .5%  
Z5U: Initial requirement + 1%  
Y5V: Initial requirement + 2%



## Mechanical

### END TERMINATION ADHERENCE

#### Specification

No evidence of peeling of end terminal

#### Measuring Conditions

After soldering devices to circuit board apply 5N (0.51kg f) for  $10 \pm 1$  seconds, please refer to Figure 1.

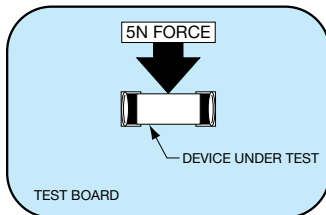


Figure 1.  
Terminal Adhesion

### RESISTANCE TO VIBRATION

#### Specification

##### Appearance:

No visual defects

##### Capacitance

Within specified tolerance

##### Q, Tan Delta

To meet initial requirement

##### Insulation Resistance

C0G (NP0), X7R  $\geq$  Initial Value  $\times 0.3$   
Z5U, Y5V  $\geq$  Initial Value  $\times 0.1$

#### Measuring Conditions

##### Vibration Frequency

10-2000 Hz

##### Maximum Acceleration

20G

##### Swing Width

1.5mm

##### Test Time

X, Y, Z axis for 2 hours each, total 6 hours of test

### SOLDERABILITY

#### Specification

$\geq 95\%$  of each termination end should be covered with fresh solder

#### Measuring Conditions

Dip device in eutectic solder at  $230 \pm 5^\circ\text{C}$  for  $2 \pm .5$  seconds

### BEND STRENGTH

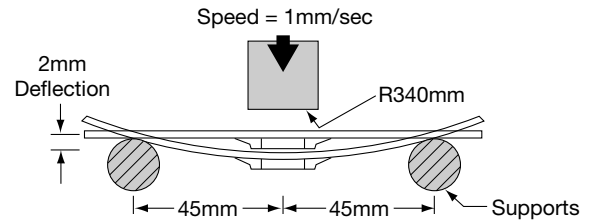


Figure 2. Bend Strength

#### Specification

##### Appearance:

No visual defects

##### Capacitance Variation

C0G (NP0):  $\pm 5\%$  or  $\pm .5\text{pF}$ , whichever is larger

X7R:  $\leq \pm 12\%$

Z5U:  $\leq \pm 30\%$

Y5V:  $\leq \pm 30\%$

##### Insulation Resistance

C0G (NP0):  $\geq$  Initial Value  $\times 0.3$

X7R:  $\geq$  Initial Value  $\times 0.3$

Z5U:  $\geq$  Initial Value  $\times 0.1$

Y5V:  $\geq$  Initial Value  $\times 0.1$

#### Measuring Conditions

Please refer to Figure 2

##### Deflection:

2mm

##### Test Time:

30 seconds

### RESISTANCE TO SOLDER HEAT

#### Specification

##### Appearance:

No serious defects,  $<25\%$  leaching of either end terminal

##### Capacitance Variation

C0G (NP0):  $\pm 2.5\%$  or  $\pm 2.5\text{pF}$ , whichever is greater

X7R:  $\leq \pm 7.5\%$

Z5U:  $\leq \pm 20\%$

Y5V:  $\leq \pm 20\%$

##### Q, Tan Delta

To meet initial requirement

##### Insulation Resistance

To meet initial requirement

##### Dielectric Strength

No problem observed

#### Measuring Conditions

Dip device in eutectic solder at  $260^\circ\text{C}$ , for 1 minute. Store at room temperature for 48 hours (24 hours for C0G (NP0)) before measuring electrical parameters.

Part sizes larger than  $3.20\text{mm} \times 2.49\text{mm}$  are reheated at  $150^\circ\text{C}$  for  $30 \pm 5$  seconds before performing test.

# European Detail Specifications CECC 32 101-801/Chips



## Standard European Ceramic Chip Capacitors

### PART NUMBER (example)

**0805**

**Size**  
(L" x W")

**5**

**Voltage**  
50V = 5  
100V = 1  
200V = 2

**C**

**Dielectric**  
1B CG = A  
2R1 = C  
2F4 = G

**103**

**Capacitance Code**

**M**

**Capacitance Tolerance**  
See Dielectrics  
COG, X7R, Y5V

**T**

**Specification**  
CECC32101-801

**T**

**Terminations**  
T = Plated Ni and Sn

**2**

**Marking Packaging**  
2 = 7" Reel  
4 = 13" Reel

**A**

**Special Code**  
A = Std. Product

### RANGE OF APPROVED COMPONENTS

Case Size	Dielectric Type	Voltage and Capacitance Range		
		50V	100V	200V
1BCG				
0603	1B CG	0.47pF - 150pF	0.47pF - 120pF	0.47pF - 100pF
0805	1B CG	0.47pF - 560pF	0.47pF - 560pF	0.47pF - 330pF
1206	1B CG	0.47pF - 3.3nF	0.47pF - 3.3nF	0.47pF - 1.5nF
1210	1B CG	0.47pF - 4.7nF	0.47pF - 4.7nF	0.47pF - 2.7nF
1808	1B CG	0.47pF - 6.8nF	0.47pF - 6.8nF	0.47pF - 4.7nF
1812	1B CG	0.47pF - 15nF	0.47pF - 15nF	0.47pF - 10nF
2220	1B CG	0.47pF - 39nF	0.47pF - 39nF	0.47pF - 15nF
2R1				
0603	2R1	10pF - 6.8nF	10pF - 6.8nF	10pF - 1.2nF
0805	2R1	10pF - 33nF	10pF - 18nF	10pF - 3.3nF
1206	2R1	10pF - 100nF	10pF - 68nF	10pF - 18nF
1210	2R1	10pF - 150nF	10pF - 100nF	10pF - 27nF
1808	2R1	10pF - 270nF	10pF - 180nF	10pF - 47nF
1812	2R1	10pF - 470nF	10pF - 330nF	10pF - 100nF
2220	2R1	10pF - 1.2μF	10pF - 680nF	10pF - 220nF
2F4				
0805	2F4	10pF - 100nF		
1206	2F4	10pF - 330nF		
1210	2F4	10pF - 470nF		
1808	2F4	10pF - 560nF		
1812	2F4	10pF - 1.8μF		
2220	2F4	10pF - 2.2μF		

# Packaging of Chip Components



## Automatic Insertion Packaging

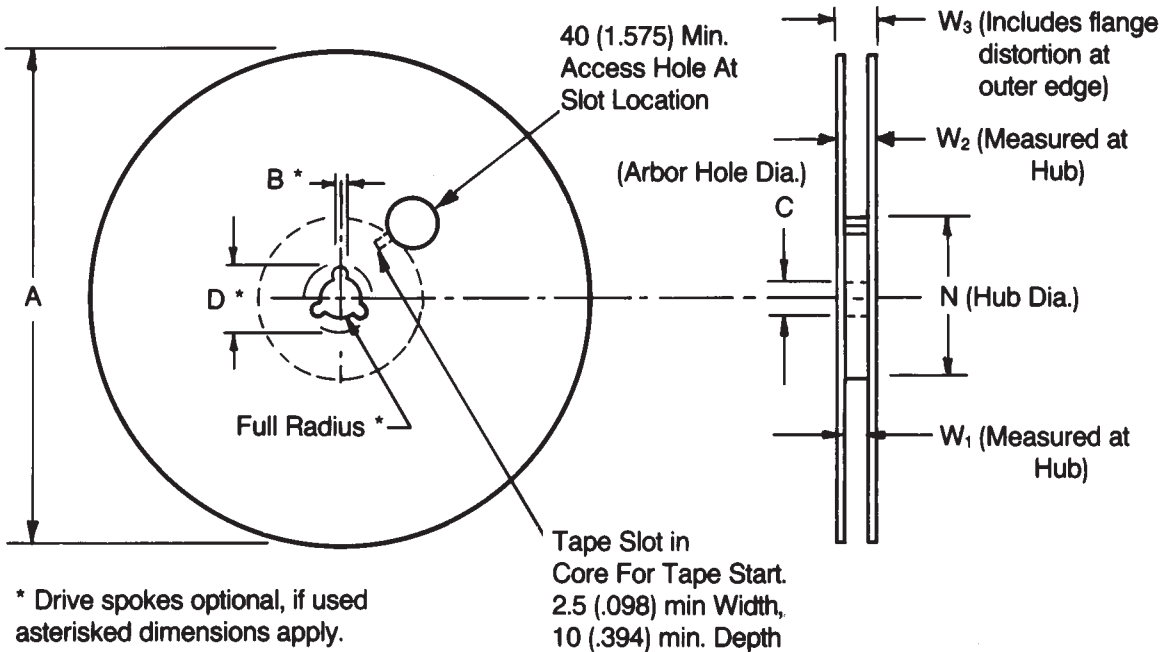
### TAPE & REEL QUANTITIES

All tape and reel specifications are in compliance with RS481.

	8mm	12mm	
Paper or Embossed Carrier	0805, 1005, 1206, 1210		
Embossed Only	0504, 0907	1505, 1805, 1808	1812, 1825, 2220, 2225
Paper Only	0402, 0603		
Qty. per Reel/7" Reel	2,000 or 4,000 <sup>(1)</sup>	3,000	1,000
Qty. per Reel/13" Reel	10,000	10,000	4,000

<sup>(1)</sup> Dependent on chip thickness. Low profile chips shown on page 27 are 5,000 per reel for 7" reel. 0402 size chips are 10,000 per 7" reels and are not available on 13" reels. For 3640 size chip contact factory for quantity per reel.

### REEL DIMENSIONS



Tape Size <sup>(1)</sup>	A Max.	B* Min.	C	D* Min.	N Min.	W <sub>1</sub>	W <sub>2</sub> Max.	W <sub>3</sub>
8mm	330 (12.992)	1.5 (.059)	13.0±0.20 (.512±.008)	20.2 (.795)	50 (1.969)	8.4 <sup>+1.0</sup> <sub>-0.0</sub> (.331 <sup>+0.60</sup> <sub>-0.0</sub> )	14.4 (.567)	7.9 Min. (.311) 10.9 Max. (.429)
12mm						12.4 <sup>+2.0</sup> <sub>-0.0</sub> (.488 <sup>+0.76</sup> <sub>-0.0</sub> )	18.4 (.724)	11.9 Min. (.469) 15.4 Max. (.607)

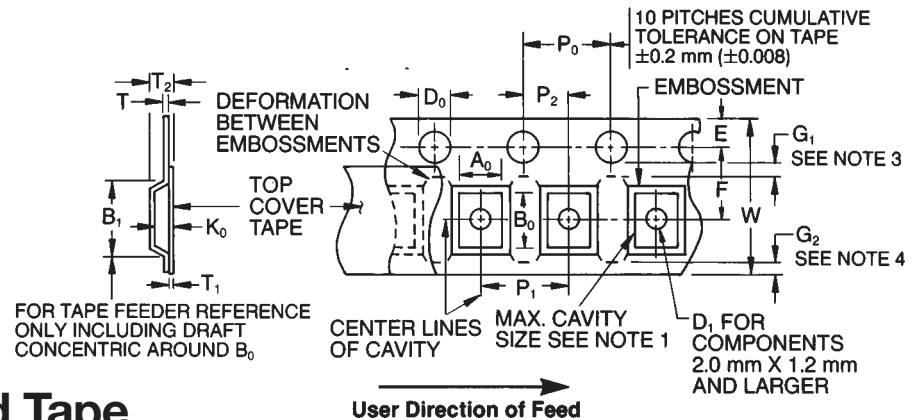
Metric dimensions will govern.  
English measurements rounded and for reference only.

<sup>(1)</sup> For tape sizes 16mm and 24mm (used with chip size 3640) consult EIA RS-481 latest revision.

# Embossed Carrier Configuration



8 & 12mm Tape Only



## 8 & 12mm Embossed Tape Metric Dimensions Will Govern

### CONSTANT DIMENSIONS

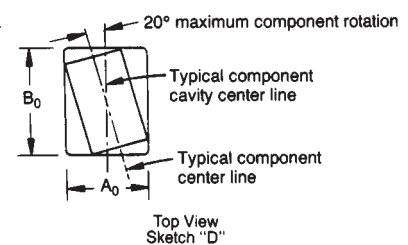
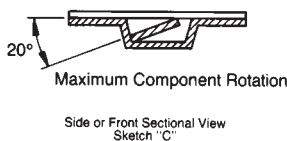
Tape Size	D <sub>0</sub>	E	P <sub>0</sub>	P <sub>2</sub>	T Max.	T <sub>1</sub>	G <sub>1</sub>	G <sub>2</sub>
8mm and 12mm	8.4 <sup>+0.10</sup> <sub>-0.0</sub> (.059 <sup>+0.004</sup> <sub>-0.0</sub> )	1.75 ± 0.10 (.069 ± .004)	4.0 ± 0.10 (.157 ± .004)	2.0 ± 0.05 (.079 ± .002)	0.600 (.024)	0.10 (.004) Max.	0.75 (.030) Min. See Note 3	0.75 (.030) Min. See Note 4

### VARIABLE DIMENSIONS

Tape Size	B <sub>1</sub> Max. See Note 6	D <sub>1</sub> Min. See Note 5	F	P <sub>1</sub>	R Min. See Note 2	T <sub>2</sub>	W	A <sub>0</sub> B <sub>0</sub> K <sub>0</sub>
8mm	4.55 (.179)	1.0 (.039)	3.5 ± 0.05 (.138 ± .002)	4.0 ± 0.10 (.157 ± .004)	25 (.984)	2.5 Max. (.098)	8.0 <sup>+0.3</sup> <sub>-0.1</sub> (.315 <sup>+0.012</sup> <sub>-.004</sub> )	See Note 1
12mm	8.2 (.323)	1.5 (.059)	5.5 ± 0.05 (.217 ± .002)	4.0 ± 0.10 (.157 ± .004)	30 (1.181)	6.5 Max. (.256)	12.0 ± .30 (.472 ± .012)	See Note 1
8mm 1/2 Pitch	4.55 (.179)	1.0 (.039)	3.5 ± 0.05 (.138 ± .002)	2.0 ± 0.10 0.79 ± .004	25 (.984)	2.5 Max. (.098)	8.0 <sup>+0.3</sup> <sub>-0.1</sub> (.315 <sup>+0.012</sup> <sub>-.004</sub> )	See Note 1
12mm Double Pitch	8.2 (.323)	1.5 (.059)	5.5 ± 0.05 (.217 ± .002)	8.0 ± 0.10 (.315 ± .004)	30 (1.181)	6.5 Max. (.256)	12.0 ± .30 (.472 ± .012)	See Note 1

#### NOTES:

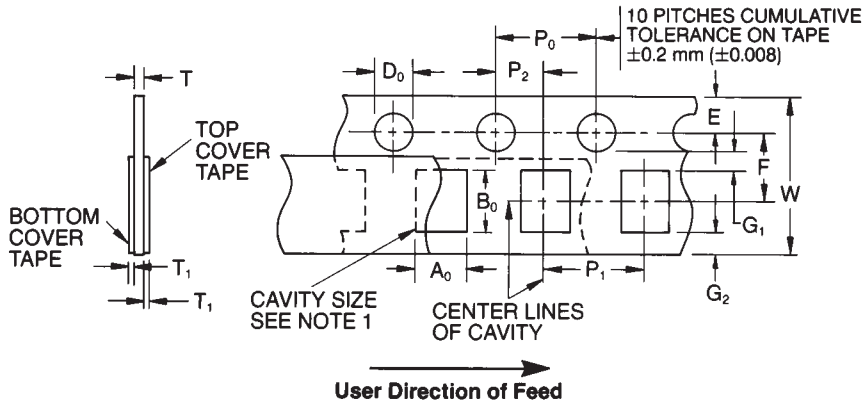
- A<sub>0</sub>, B<sub>0</sub>, and K<sub>0</sub> are determined by the max. dimensions to the ends of the terminals extending from the component body and/or the body dimensions of the component. The clearance between the end of the terminals or body of the component to the sides and depth of the cavity (A<sub>0</sub>, B<sub>0</sub>, and K<sub>0</sub>) must be within 0.05 mm (.002) min. and 0.50 mm (.020) max. The clearance allowed must also prevent rotation of the component within the cavity of not more than 20 degrees (see sketches C & D).
- Tape with components shall pass around radius "R" without damage. The minimum trailer length (Note 2 Fig. 3) may require additional length to provide R min. for 12 mm embossed tape for reels with hub diameters approaching N min. (Table 4).
- G<sub>1</sub> dimension is the flat area from the edge of the sprocket hole to either the outward deformation of the carrier tape between the embossed cavities or to the edge of the cavity whichever is less.
- G<sub>2</sub> dimension is the flat area from the edge of the carrier tape opposite the sprocket holes to either the outward deformation of the carrier tape between the embossed cavity or to the edge of the cavity whichever is less.
- The embossment hole location shall be measured from the sprocket hole controlling the location of the embossment. Dimensions of embossment location and hole location shall be applied independent of each other.
- B<sub>1</sub> dimension is a reference dimension for tape feeder clearance only.



# Paper Carrier Configuration



8 & 12mm Tape Only



## 8 & 12mm Paper Tape Metric Dimensions Will Govern

### CONSTANT DIMENSIONS

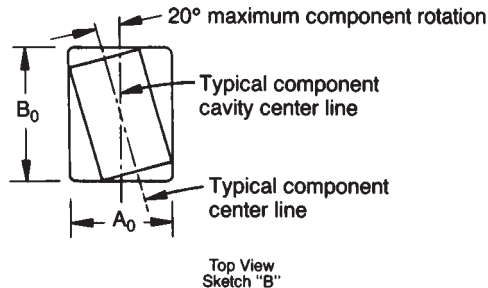
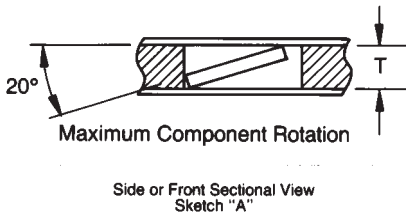
Tape Size	D <sub>0</sub>	E	P <sub>0</sub>	P <sub>2</sub>	T <sub>1</sub>	G <sub>1</sub>	G <sub>2</sub>	R MIN.
8mm and 12mm	1.5 <sup>+0.1</sup> <sub>-0.0</sub> (.059 <sup>+0.004</sup> <sub>-.000</sub> )	1.75 ± 0.10 (.069 ± .004)	4.0 ± 0.10 (.157 ± .004)	2.0 ± 0.05 (.079 ± .002)	0.10 (.004) Max.	0.75 (.030) Min.	0.75 (.030) Min.	25 (.984) See Note 2

### VARIABLE DIMENSIONS

Tape Size	P <sub>1</sub>	F	W	A <sub>0</sub> B <sub>0</sub>	T
8mm	4.0 ± 0.10 (.157 ± .004)	3.5 ± 0.05 (.138 ± .002)	8.0 <sup>+0.3</sup> <sub>-0.1</sub> (.315 <sup>+0.012</sup> <sub>-.004</sub> )	See Note 1	See Note 3
12mm	4.0 ± .010 (.157 ± .004)	5.5 ± 0.05 (.217 ± .002)	12.0 ± 0.3 (.472 ± .012)		
8mm 1/2 Pitch	2.0 ± 0.10 (.079 ± .004)	3.5 ± 0.05 (.138 ± .002)	8.0 <sup>+0.3</sup> <sub>-0.1</sub> (.315 <sup>+0.012</sup> <sub>-.004</sub> )		
12mm Double Pitch	8.0 ± 0.10 (.315 ± .004)	5.5 ± 0.05 (.217 ± .002)	12.0 ± 0.3 (.472 ± .012)		

#### NOTES:

1. A<sub>0</sub>, B<sub>0</sub>, and T are determined by the max. dimensions to the ends of the terminals extending from the component body and/or the body dimensions of the component. The clearance between the ends of the terminals or body of the component to the sides and depth of the cavity (A<sub>0</sub>, B<sub>0</sub>, and T) must be within 0.05 mm (.002) min. and 0.50 mm (.020) max. The clearance allowed must also prevent rotation of the component within the cavity of not more than 20 degrees (see sketches A & B).
2. Tape with components shall pass around radius "R" without damage.
3. 1.1 mm (.043) Base Tape and 1.6 mm (.063) Max. for Non-Paper Base Compositions.



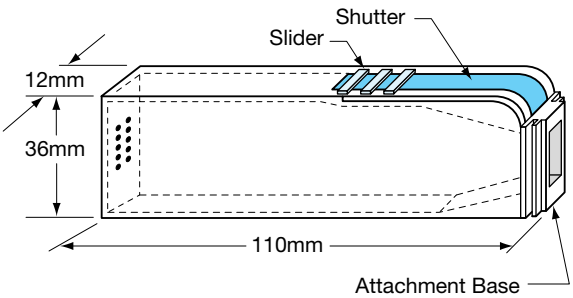
## Bar Code Labeling Standard

AVX bar code labeling is available and follows latest version of EIA-556-A.

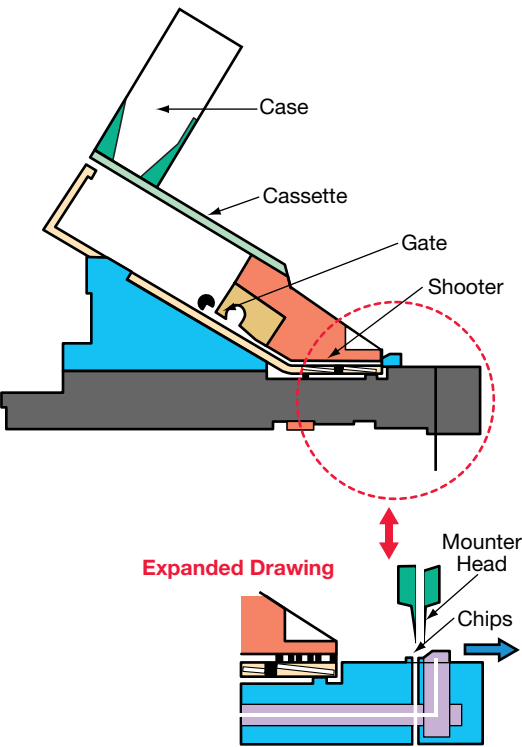
## BENEFITS

- Easier handling
- Smaller packaging volume  
(1/20 of T/R packaging)
- Easier inventory control
- Flexibility
- Recyclable

## CASE DIMENSIONS



## BULK FEEDER

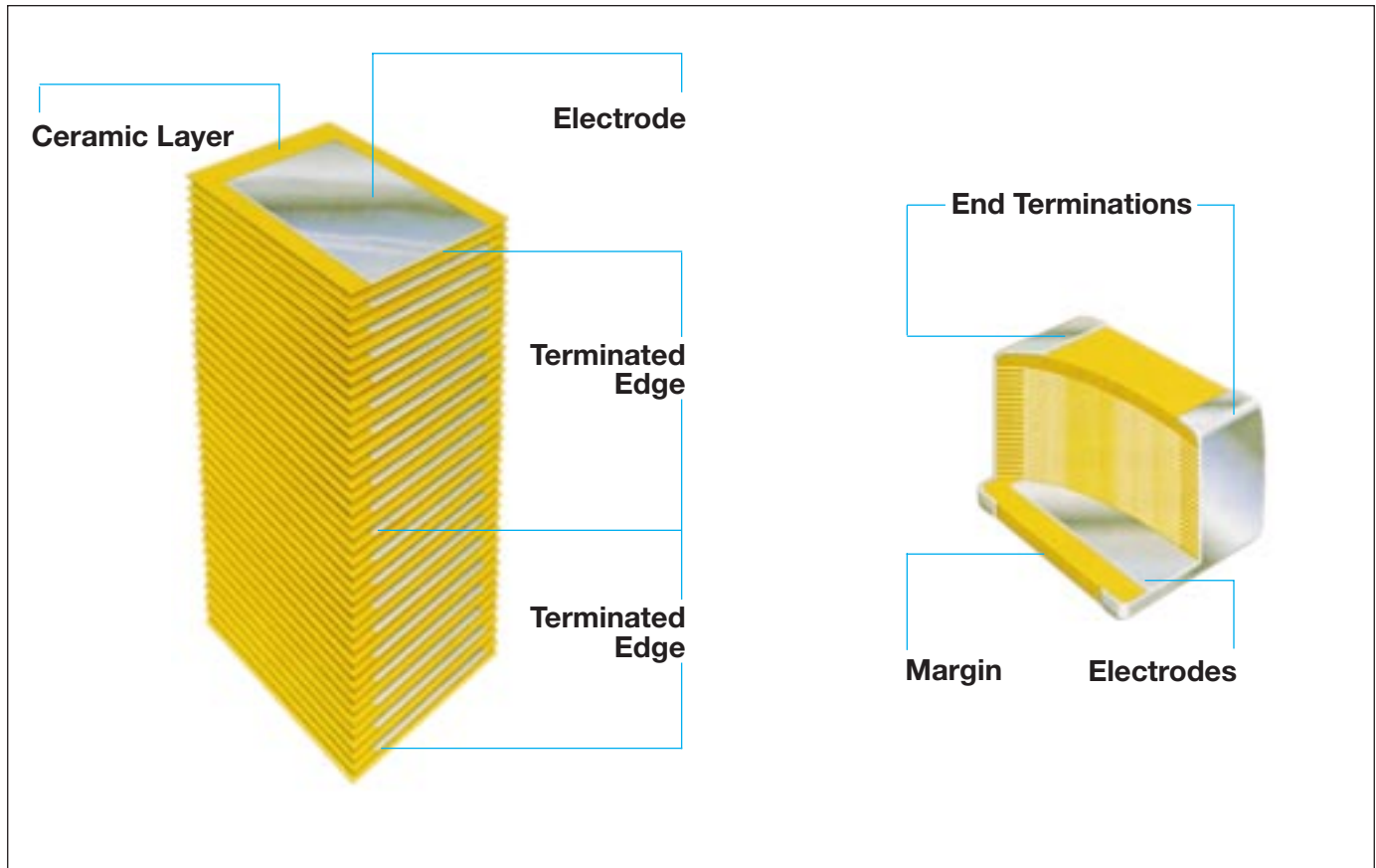


## CASE QUANTITIES

Part Size	0402	0603	0805
Qty. (pcs / cassette)	80,000	15,000	10,000 (T=0.6mm) 5,000 (T≥0.6mm)

**Basic Construction** – A multilayer ceramic (MLC) capacitor is a monolithic block of ceramic containing two sets of offset, interleaved planar electrodes that extend to two opposite surfaces of the ceramic dielectric. This simple

structure requires a considerable amount of sophistication, both in material and manufacture, to produce it in the quality and quantities needed in today's electronic equipment.



**Formulations** – Multilayer ceramic capacitors are available in both Class 1 and Class 2 formulations. Temperature compensating formulations are Class 1 and temperature stable and general application formulations are classified as Class 2.

**Class 1** – Class 1 capacitors or temperature compensating capacitors are usually made from mixtures of titanates where barium titanate is normally not a major part of the mix. They have predictable temperature coefficients and in general, do not have an aging characteristic. Thus they are the most stable capacitor available. The most popular Class 1 multilayer ceramic capacitors are C0G (NP0) temperature compensating capacitors (negative-positive 0 ppm/°C).

**Class 2** – EIA Class 2 capacitors typically are based on the chemistry of barium titanate and provide a wide range of capacitance values and temperature stability. The most commonly used Class 2 dielectrics are X7R and Y5V. The X7R provides intermediate capacitance values which vary only  $\pm 15\%$  over the temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . It finds applications where stability over a wide temperature range is required.

The Y5V provides the highest capacitance values and is used in applications where limited temperature changes are expected. The capacitance value for Y5V can vary from 22% to -82% over the  $-30^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  temperature range. The Z5U dielectric is between X7R and Y5V in both stability and capacitance range.

All Class 2 capacitors vary in capacitance value under the influence of temperature, operating voltage (both AC and DC), and frequency. For additional information on performance changes with operating conditions, consult AVX's software, SpiCap.

**Effects of Voltage** – Variations in voltage have little effect on Class 1 dielectric but does affect the capacitance and dissipation factor of Class 2 dielectrics. The application of DC voltage reduces both the capacitance and dissipation factor while the application of an AC voltage within a reasonable range tends to increase both capacitance and dissipation factor readings. If a high enough AC voltage is applied, eventually it will reduce capacitance just as a DC voltage will. Figure 2 shows the effects of AC voltage.

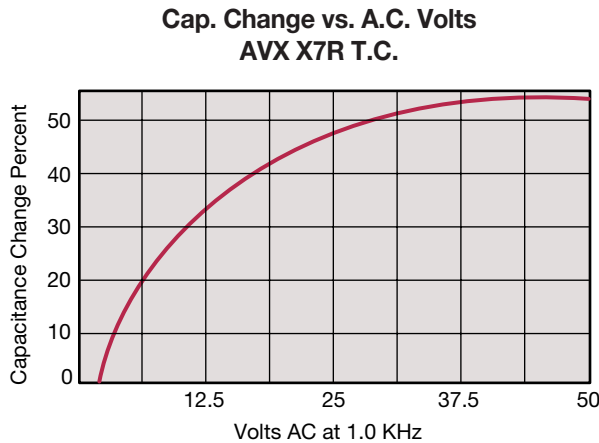


Figure 2

Capacitor specifications specify the AC voltage at which to measure (normally 0.5 or 1 VAC) and application of the wrong voltage can cause spurious readings. Figure 3 gives the voltage coefficient of dissipation factor for various AC voltages at 1 kilohertz. Applications of different frequencies will affect the percentage changes versus voltages.

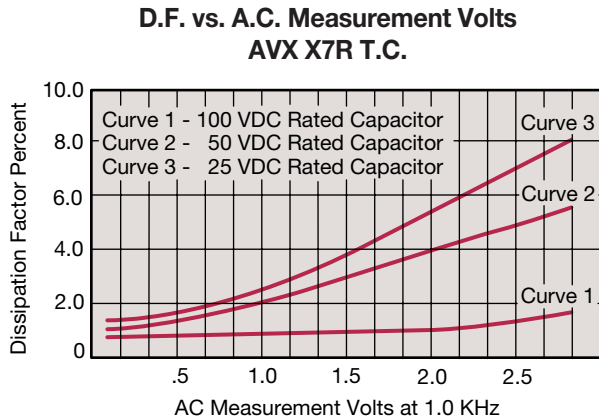


Figure 3

The effect of the application of DC voltage is shown in Figure 4. The voltage coefficient is more pronounced for higher K dielectrics. These figures are shown for room temperature conditions. The combination characteristic known as voltage temperature limits which shows the effects of rated voltage over the operating temperature range is shown in Figure 5 for the military BX characteristic.

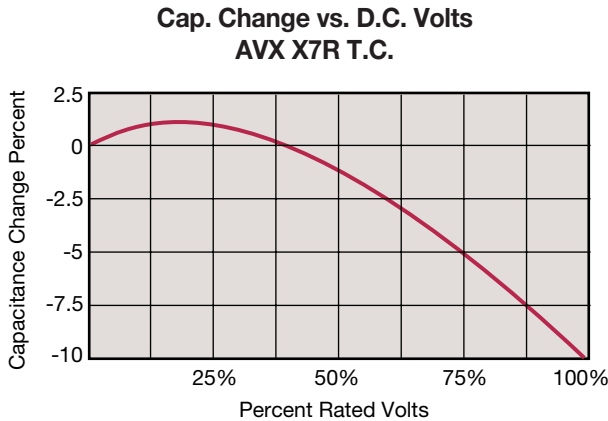


Figure 4

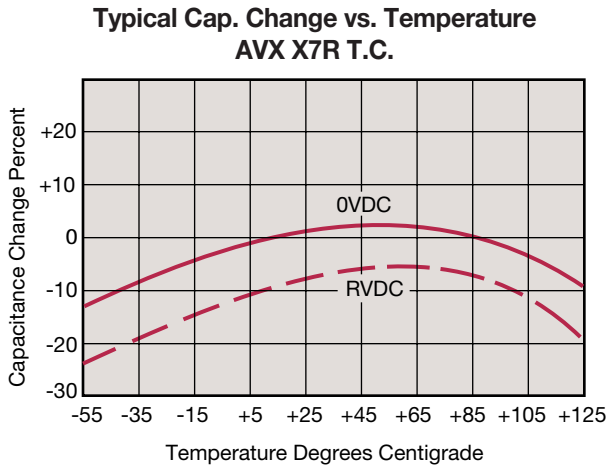


Figure 5

**Effects of Time** – Class 2 ceramic capacitors change capacitance and dissipation factor with time as well as temperature, voltage and frequency. This change with time is known as aging. Aging is caused by a gradual re-alignment of the crystalline structure of the ceramic and produces an exponential loss in capacitance and decrease in dissipation factor versus time. A typical curve of aging rate for semi-stable ceramics is shown in Figure 6.

If a Class 2 ceramic capacitor that has been sitting on the shelf for a period of time, is heated above its curie point, (125°C for 4 hours or 150°C for ½ hour will suffice) the part will de-age and return to its initial capacitance and dissipation factor readings. Because the capacitance changes rapidly, immediately after de-aging, the basic capacitance measurements are normally referred to a time period sometime after the de-aging process. Various manufacturers use different time bases but the most popular one is one day or twenty-four hours after “last heat.” Change in the aging curve can be caused by the application of voltage and other stresses. The possible changes in capacitance due to de-aging by heating the unit explain why capacitance changes are allowed after test, such as temperature cycling, moisture resistance, etc., in MIL specs. The application of high voltages such as dielectric withstanding voltages also





# General Description



**Energy Stored** – The energy which can be stored in a capacitor is given by the formula:

$$E = \frac{1}{2}CV^2$$

**E** = energy in joules (watts-sec)

**V** = applied voltage

**C** = capacitance in farads

**Potential Change** – A capacitor is a reactive component which reacts against a change in potential across it. This is shown by the equation for the linear charge of a capacitor:

$$I_{ideal} = C \frac{dV}{dt}$$

where

**I** = Current

**C** = Capacitance

**dV/dt** = Slope of voltage transition across capacitor

Thus an infinite current would be required to instantly change the potential across a capacitor. The amount of current a capacitor can “sink” is determined by the above equation.

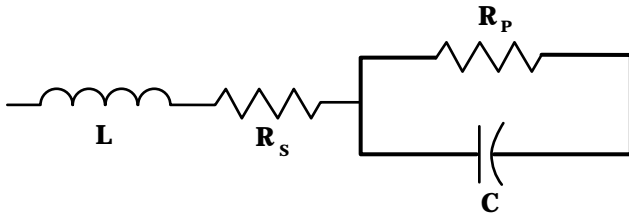
**Equivalent Circuit** – A capacitor, as a practical device, exhibits not only capacitance but also resistance and inductance. A simplified schematic for the equivalent circuit is:

**C** = Capacitance

**L** = Inductance

**R<sub>s</sub>** = Series Resistance

**R<sub>p</sub>** = Parallel Resistance



**Reactance** – Since the insulation resistance (**R<sub>p</sub>**) is normally very high, the total impedance of a capacitor is:

$$Z = \sqrt{R_s^2 + (X_c - X_L)^2}$$

where

**Z** = Total Impedance

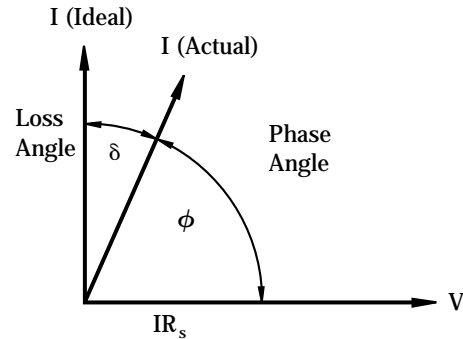
**R<sub>s</sub>** = Series Resistance

**X<sub>c</sub>** = Capacitive Reactance =  $\frac{1}{2\pi fC}$

**X<sub>L</sub>** = Inductive Reactance =  $2\pi fL$

The variation of a capacitor's impedance with frequency determines its effectiveness in many applications.

**Phase Angle** – Power Factor and Dissipation Factor are often confused since they are both measures of the loss in a capacitor under AC application and are often almost identical in value. In a “perfect” capacitor the current in the capacitor will lead the voltage by 90°.



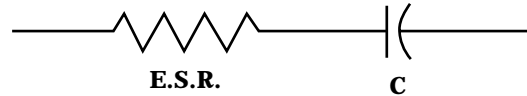
In practice the current leads the voltage by some other phase angle due to the series resistance **R<sub>s</sub>**. The complement of this angle is called the loss angle and:

Power Factor (P.F.) =  $\cos \phi$  or  $\sin \delta$

Dissipation Factor (D.F.) =  $\tan \delta$

for small values of  $\delta$  the tan and sine are essentially equal which has led to the common interchangeability of the two terms in the industry.

**Equivalent Series Resistance** – The term E.S.R. or Equivalent Series Resistance combines all losses both series and parallel in a capacitor at a given frequency so that the equivalent circuit is reduced to a simple R-C series connection.



**Dissipation Factor** – The DF/PF of a capacitor tells what percent of the apparent power input will turn to heat in the capacitor.

$$\text{Dissipation Factor} = \frac{\text{E.S.R.}}{X_c} = (2\pi fC) (\text{E.S.R.})$$

The watts loss are:

$$\text{Watts loss} = (2\pi fCV^2) (\text{D.F.})$$

Very low values of dissipation factor are expressed as their reciprocal for convenience. These are called the “Q” or Quality factor of capacitors.

**Parasitic Inductance** – The parasitic inductance of capacitors is becoming more and more important in the decoupling of today's high speed digital systems. The relationship between the inductance and the ripple voltage induced on the DC voltage line can be seen from the simple inductance equation:

$$V = L \frac{di}{dt}$$

The  $\frac{di}{dt}$  seen in current microprocessors can be as high as 0.3 A/ns, and up to 10A/ns. At 0.3 A/ns, 100pH of parasitic inductance can cause a voltage spike of 30mV. While this does not sound very drastic, with the Vcc for microprocessors decreasing at the current rate, this can be a fairly large percentage.

Another important, often overlooked, reason for knowing the parasitic inductance is the calculation of the resonant frequency. This can be important for high frequency, bypass capacitors, as the resonant point will give the most signal attenuation. The resonant frequency is calculated from the simple equation:

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}$$

**Insulation Resistance** – Insulation Resistance is the resistance measured across the terminals of a capacitor and consists principally of the parallel resistance  $R_P$  shown in the equivalent circuit. As capacitance values and hence the area of dielectric increases, the I.R. decreases and hence the product (C x IR or RC) is often specified in ohm farads or more commonly megohm-microfarads. Leakage current

is determined by dividing the rated voltage by IR (Ohm's Law).

**Dielectric Strength** – Dielectric Strength is an expression of the ability of a material to withstand an electrical stress. Although dielectric strength is ordinarily expressed in volts, it is actually dependent on the thickness of the dielectric and thus is also more generically a function of volts/mil.

**Dielectric Absorption** – A capacitor does not discharge instantaneously upon application of a short circuit, but drains gradually after the capacitance proper has been discharged. It is common practice to measure the dielectric absorption by determining the "reappearing voltage" which appears across a capacitor at some point in time after it has been fully discharged under short circuit conditions.

**Corona** – Corona is the ionization of air or other vapors which causes them to conduct current. It is especially prevalent in high voltage units but can occur with low voltages as well where high voltage gradients occur. The energy discharged degrades the performance of the capacitor and can in time cause catastrophic failures.

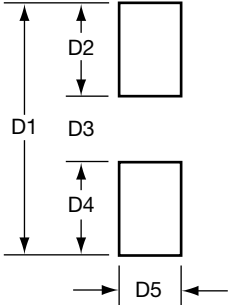
## MLC Chip Capacitors

### Component Pad Design

Component pads should be designed to achieve good solder filets and minimize component movement during reflow soldering. Pad designs are given below for the most common sizes of multilayer ceramic capacitors for both wave and reflow soldering. The basis of these designs is:

- Pad width equal to component width. It is permissible to decrease this to as low as 85% of component width but it is not advisable to go below this.
- Pad overlap 0.5mm beneath component.
- Pad extension 0.5mm beyond components for reflow and 1.0mm for wave soldering.

### REFLOW SOLDERING

 <p>Dimensions in millimeters (inches)</p>	Case Size	D1	D2	D3	D4	D5
	0402	1.70 (0.07)	0.60 (0.02)	0.50 (0.02)	0.60 (0.02)	0.50 (0.02)
	0603	2.30 (0.09)	0.80 (0.03)	0.70 (0.03)	0.80 (0.03)	0.75 (0.03)
	0805	3.00 (0.12)	1.00 (0.04)	1.00 (0.04)	1.00 (0.04)	1.25 (0.05)
	1206	4.00 (0.16)	1.00 (0.04)	2.00 (0.09)	1.00 (0.04)	1.60 (0.06)
	1210	4.00 (0.16)	1.00 (0.04)	2.00 (0.09)	1.00 (0.04)	2.50 (0.10)
	1808	5.60 (0.22)	1.00 (0.04)	3.60 (0.14)	1.00 (0.04)	2.00 (0.08)
	1812	5.60 (0.22)	1.00 (0.04))	3.60 (0.14)	1.00 (0.04)	3.00 (0.12)
	1825	5.60 (0.22)	1.00 (0.04)	3.60 (0.14)	1.00 (0.04)	6.35 (0.25)
	2220	6.60 (0.26)	1.00 (0.04)	4.60 (0.18)	1.00 (0.04)	5.00 (0.20)
	2225	6.60 (0.26)	1.00 (0.04)	4.60 (0.18)	1.00 (0.04)	6.35 (0.25)

# Surface Mounting Guide



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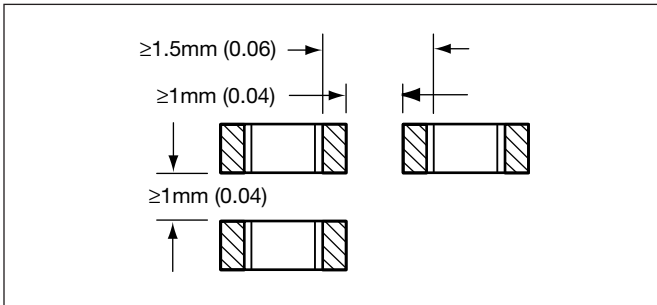
### WAVE SOLDERING

	Case Size	D1	D2	D3	D4	D5
	0603	3.10 (0.12)	1.20 (0.05)	0.70 (0.03)	1.20 (0.05)	0.75 (0.03)
	0805	4.00 (0.15)	1.50 (0.06)	1.00 (0.04)	1.50 (0.06)	1.25 (0.05)
	1206	5.00 (0.19)	1.50 (0.06)	2.00 (0.09)	1.50 (0.06)	1.60 (0.06)
	1210	5.00 (0.19)	1.50 (0.06)	2.00 (0.09)	1.50 (0.06)	2.50 (0.10)

Dimensions in millimeters (inches)

#### Component Spacing

For wave soldering components, must be spaced sufficiently far apart to avoid bridging or shadowing (inability of solder to penetrate properly into small spaces). This is less important for reflow soldering but sufficient space must be allowed to enable rework should it be required.



#### Preheat & Soldering

The rate of preheat should not exceed 4°C/second to prevent thermal shock. A better maximum figure is about 2°C/second.

For capacitors size 1206 and below, with a maximum thickness of 1.25mm, it is generally permissible to allow a temperature differential from preheat to soldering of 150°C. In all other cases this differential should not exceed 100°C.

For further specific application or process advice, please consult AVX.

#### Cleaning

Care should be taken to ensure that the capacitors are thoroughly cleaned of flux residues especially the space beneath the capacitor. Such residues may otherwise become conductive and effectively offer a low resistance bypass to the capacitor.

Ultrasonic cleaning is permissible, the recommended conditions being 8 Watts/litre at 20-45 kHz, with a process cycle of 2 minutes vapor rinse, 2 minutes immersion in the ultrasonic solvent bath and finally 2 minutes vapor rinse.

# Surface Mounting Guide



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### APPLICATION NOTES

#### Storage

Good solderability is maintained for at least twelve months, provided the components are stored in their "as received" packaging at less than 40°C and 70% RH.

#### Solderability

Terminations to be well soldered after immersion in a 60/40 tin/lead solder bath at 235 ±5°C for 2±1 seconds.

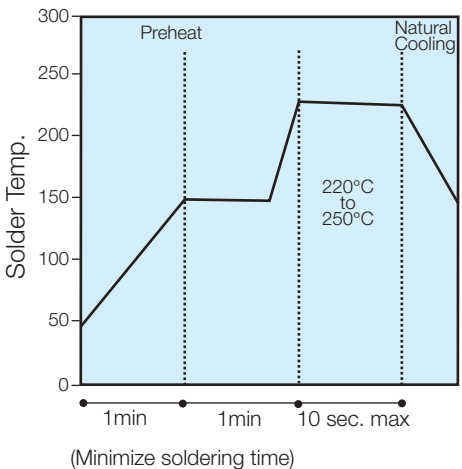
#### Leaching

Terminations will resist leaching for at least the immersion times and conditions shown below.

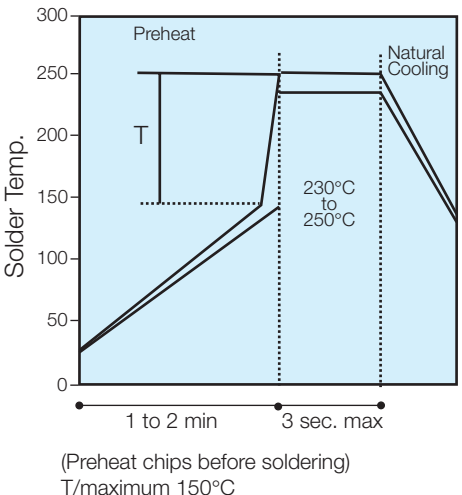
Termination Type	Solder Tin/Lead/Silver	Solder Temp. °C	Immersion Time Seconds
Nickel Barrier	60/40/0	260±5	30±1

### Recommended Soldering Profiles

#### Reflow



#### Wave



#### General

Surface mounting chip multilayer ceramic capacitors are designed for soldering to printed circuit boards or other substrates. The construction of the components is such that they will withstand the time/temperature profiles used in both wave and reflow soldering methods.

#### Handling

Chip multilayer ceramic capacitors should be handled with care to avoid damage or contamination from perspiration and skin oils. The use of tweezers or vacuum pick ups is strongly recommended for individual components. Bulk handling should ensure that abrasion and mechanical shock are minimized. Taped and reeled components provides the ideal medium for direct presentation to the placement machine. Any mechanical shock should be minimized during handling chip multilayer ceramic capacitors.

#### Preheat

It is important to avoid the possibility of thermal shock during soldering and carefully controlled preheat is therefore required. The rate of preheat should not exceed 4°C/second and a target figure 2°C/second is recommended. Although an 80°C to 120°C temperature differential is preferred, recent developments allow a temperature differential between the component surface and the soldering temperature of 150°C (Maximum) for capacitors of 1210 size and below with a maximum thickness of 1.25mm. The user is cautioned that the risk of thermal shock increases as chip size or temperature differential increases.

#### Soldering

Mildly activated rosin fluxes are preferred. The minimum amount of solder to give a good joint should be used. Excessive solder can lead to damage from the stresses caused by the difference in coefficients of expansion between solder, chip and substrate. AVX terminations are suitable for all wave and reflow soldering systems. If hand soldering cannot be avoided, the preferred technique is the utilization of hot air soldering tools.

#### Cooling

Natural cooling in air is preferred, as this minimizes stresses within the soldered joint. When forced air cooling is used, cooling rate should not exceed 4°C/second. Quenching is not recommended but if used, maximum temperature differentials should be observed according to the preheat conditions above.

#### Cleaning

Flux residues may be hygroscopic or acidic and must be removed. AVX MLC capacitors are acceptable for use with all of the solvents described in the specifications MIL-STD-202 and EIA-RS-198. Alcohol based solvents are acceptable and properly controlled water cleaning systems are also acceptable. Many other solvents have been proven successful, and most solvents that are acceptable to other components on circuit assemblies are equally acceptable for use with ceramic capacitors.