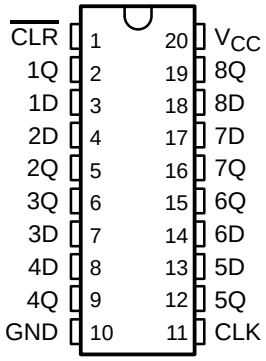
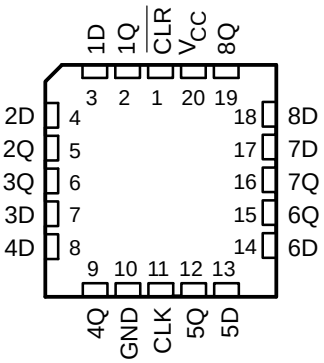
- **Operating Range 2-V to 5.5-V $V_{CC}$**
- **Contain Eight Flip-Flops With Single-Rail Outputs**
- **Direct Clear Input**
- **Individual Data Input to Each Flip-Flop**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **1000-V Charged-Device Model (C101)**

**SN54AHC273 . . . J OR W PACKAGE**
**SN74AHC273 . . . DB, DGV, DW, N, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC273 . . . FK PACKAGE**
**(TOP VIEW)**




## description

These circuits are positive-edge-triggered D-type flip-flops with a direct clear ($\overline{CLR}$) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

**ORDERING INFORMATION**

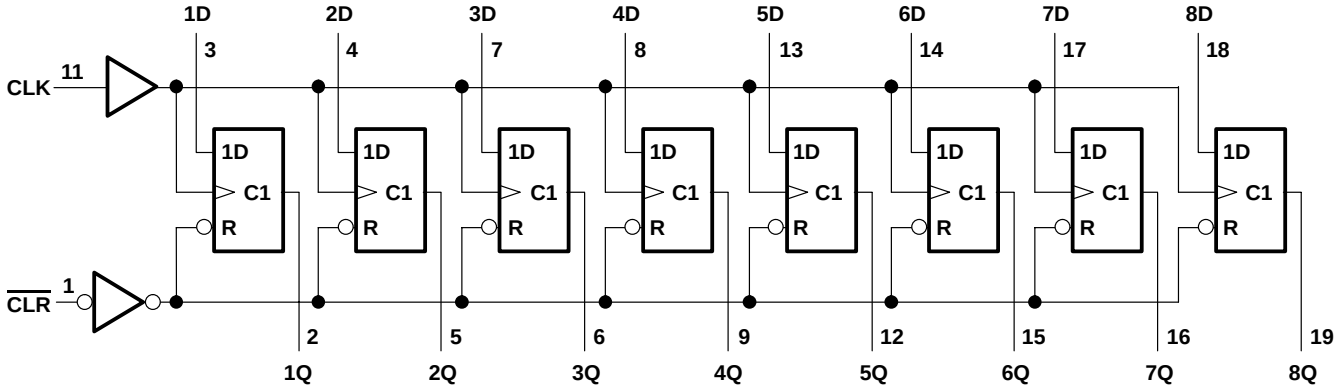
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | PDIP – N | Tube | SN74AHC273N | SN74AHC273N |
| | SOIC – DW | Tube | SN74AHC273DW | AHC273 |
| | | Tape and reel | SN74AHC273DWR | |
| | SOP – NS | Tape and reel | SN74AHC273NSR | AHC273 |
| | SSOP – DB | Tape and reel | SN74AHC273DBR | HA273 |
| | TSSOP – PW | Tape and reel | SN74AHC273PWR | HA273 |
| | TVSOP – DGV | Tape and reel | SN74AHC273DGVR | HA273 |
| –55°C to 125°C | CDIP – J | Tube | SNJ54AHC273J | SNJ54AHC273J |
| | CFP – W | Tube | SNJ54AHC273W | SNJ54AHC273W |
| | LCCC – FK | Tube | SNJ54AHC273FK | SNJ54AHC273FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

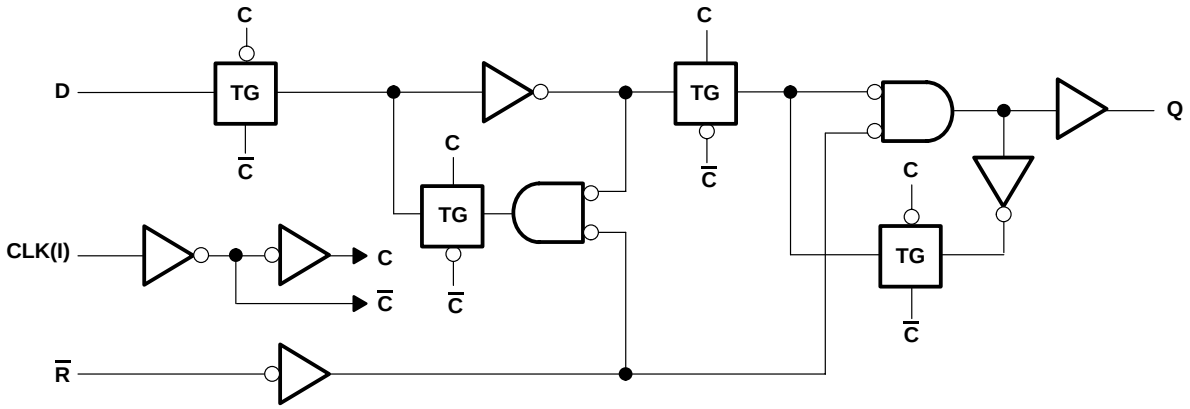
**FUNCTION TABLE**
**(each flip-flop)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{CLR}$ | CLK | D | Q |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | $Q_0$ |

## logic diagram (positive logic)




## logic diagram, each flip-flop (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . 70°C/W
DGV package . . . . . 92°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
PW package . . . . . 83°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

| | | | SN54AHC273 | | SN74AHC273 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC273 | | SN74AHC273 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1* | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 2.5 | 10 | | | | 10 | pF |

* On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC}$ = 0 V.

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| | | | SN54AHC273 | | | | SN74AHC273 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | MIN | MAX | | | |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 5 | | 6 | | 5 | | 6 | | ns |
| | | CLK high or low | 5 | | 6.5 | | 5 | | 6.5 | | |
| $t_{su}$ | Setup time | Data before CLK↑ | 5.5 | | 6.5 | | 5.5 | | 6.5 | | ns |
| | | $\overline{CLR}$ before CLK↑ | 2.5 | | 2.5 | | 2.5 | | 2.5 | | |
| $t_h$ | Hold time, data after CLK↑ | | 1.5 | | 2 | | 1 | | 1 | | ns |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | | SN54AHC273 | | | | SN74AHC273 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | MIN | MAX | $T_A$ = 25°C | | MIN | MAX | |
| | | | MIN | MAX | | | MIN | MAX | | | |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 5 | | 5 | | 5 | | 5 | | ns |
| | | CLK high or low | 5 | | 5 | | 5 | | 5 | | |
| $t_{su}$ | Setup time | Data before CLK↑ | 4.5 | | 4.5 | | 4.5 | | 4.5 | | ns |
| | | $\overline{CLR}$ before CLK↑ | 2 | | 2 | | 2 | | 2 | | |
| $t_h$ | Hold time, data after CLK↑ | | 1.5 | | 2 | | 1 | | 1 | | ns |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC273 | | SN74AHC273 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 75* | 120* | | 65* | | 65 | | MHz |
| | | | $C_L$ = 50 pF | 50 | 75 | | 45 | | 45 | | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 8.9* | 13.6* | 1* | 16* | 1 | 16 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 8.7* | 13.6* | 1* | 16* | 1 | 16 | ns |
| $t_{PHL}$ | | | | | 8.7* | 13.6* | 1* | 16* | 1 | 16 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 50 pF | | 11.4 | 17.1 | 1 | 19.5 | 1 | 19.5 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 11.2 | 17.1 | 1 | 19.5 | 1 | 19.5 | ns |
| $t_{PHL}$ | | | | | 11.2 | 17.1 | 1 | 19.5 | 1 | 19.5 | |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 1.5** | | | | 1.5 | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
** On products compliant to MIL-PRF-38535, this parameter does not apply.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC273 | | SN74AHC273 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 120* | 165* | | 100* | | 100 | | MHz |
| | | | $C_L$ = 50 pF | 80 | 110 | | 70 | | 70 | | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 15 pF | | 5.2* | 8.5* | 1* | 10* | 1 | 10 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 15 pF | | 5.8* | 9* | 1* | 10.5* | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 5.8* | 9* | 1* | 10.5* | 1 | 10.5 | |
| $t_{PHL}$ | $\overline{CLR}$ | Q | $C_L$ = 50 pF | | 6.7 | 10.5 | 1 | 12 | 1 | 12 | ns |
| $t_{PLH}$ | CLK | Q | $C_L$ = 50 pF | | 7.3 | 11 | 1 | 12.5 | 1 | 12.5 | ns |
| $t_{PHL}$ | | | | | 7.3 | 11 | 1 | 12.5 | 1 | 12.5 | |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 1** | | | | 1 | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
** On products compliant to MIL-PRF-38535, this parameter does not apply.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

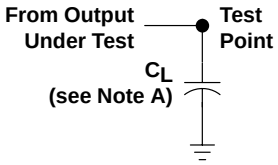
| PARAMETER | | SN74AHC273 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.7 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.7 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 4.7 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

NOTE 4: Characteristics are for surface-mount packages only.

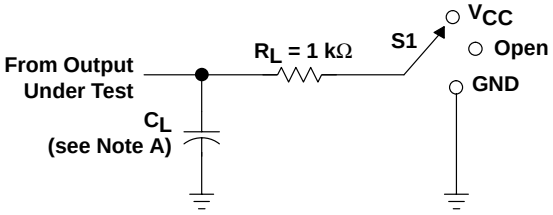
### operating characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, f = 1 MHz | 31 | pF |

## PARAMETER MEASUREMENT INFORMATION

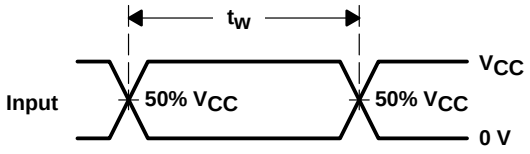



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

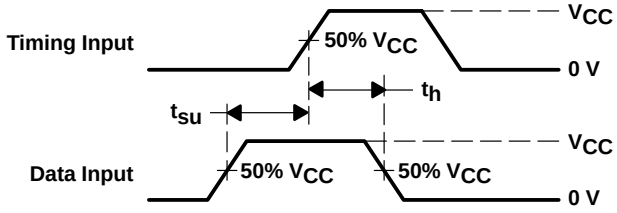



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

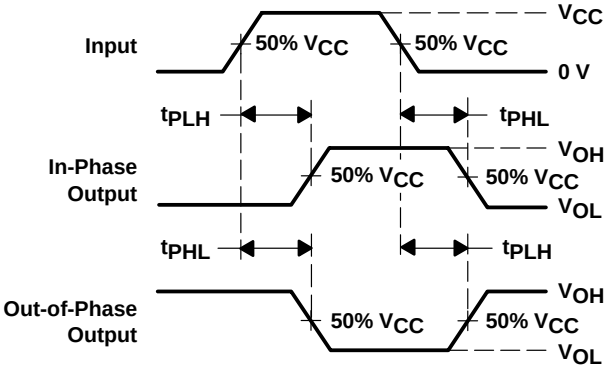
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



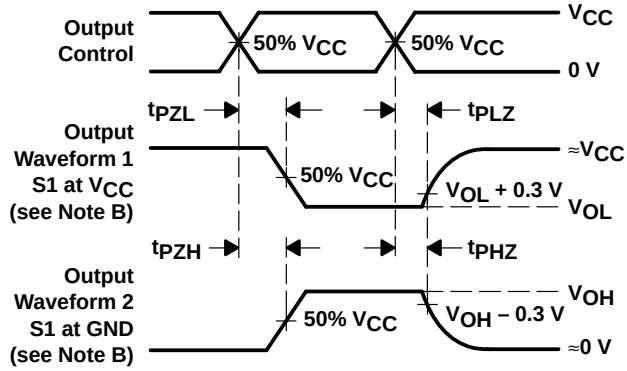

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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