

Tattletale Model 8

OPERATION MANUAL ADDENDUM

for the
TT8-V2
and the
TT8-IM-V2

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INTRODUCTION

This manual is an addendum to the Tattletale Model 8 Installation and Operation Manual that describes the differences between standard Model 8 and the newest member of the Tattletale family, the TT8V2 and TT8-1M-V2, which is the first version to include pin and socket connections for all the IIO bus connections. It also describes the new prototype board designed to mate with the TT8-V2's new pin and sockets.

Since the first TT8 was built we have had requests for a pin and socket version of the TT8. This was mostly because elastomerics were unfamiliar to many of our customers and they were concerned about the ruggedness and reliability.

Although the SquishyBus elastomeric connectors have proven themselves reliable over the years, customers continue to say they feel more comfortable with pin and sockets. More recently we have had issues with the SquishyBus connector's cost and availability. Recently gold foil elastomeric connectors have become less popular and therefore more difficult to obtain, with fewer vendors supplying them.

There were two primary design goals in creating the TT8-V2. The first was to eliminate the SquishyBus elastomeric connectors in favor of stackable pin and socket connectors. The second was to make this modification with as little impact on the TT8 form factor, layout and electrical design as possible. Since the beginning the TT8 has proven itself to be extremely rugged and reliable. Many customers have used the TT8 as the heart and soul of many complex and critical pieces of instrumentation, from medical equipment to unmanned aircraft control to instrumentation launched into space. In speaking to these customers it was clear that this would be important minimize the effort needed to new version into their existing equipment, and to minimize risks that may be introduced through component or layout changes.

Both goals were met. The TT8-V2 uses the same schematic layout and physical component layout as the previous versions. The board outline remains exactly the same. The pin and socket connectors were placed into the same area as the squishybus pads.

Needless to say we will continue to support the TT8 and the TT8-1M, but we strongly recommend that the TT8-V2 and TT8-1M-V2 be used for all new designs.

BOARD DIMENSIONS

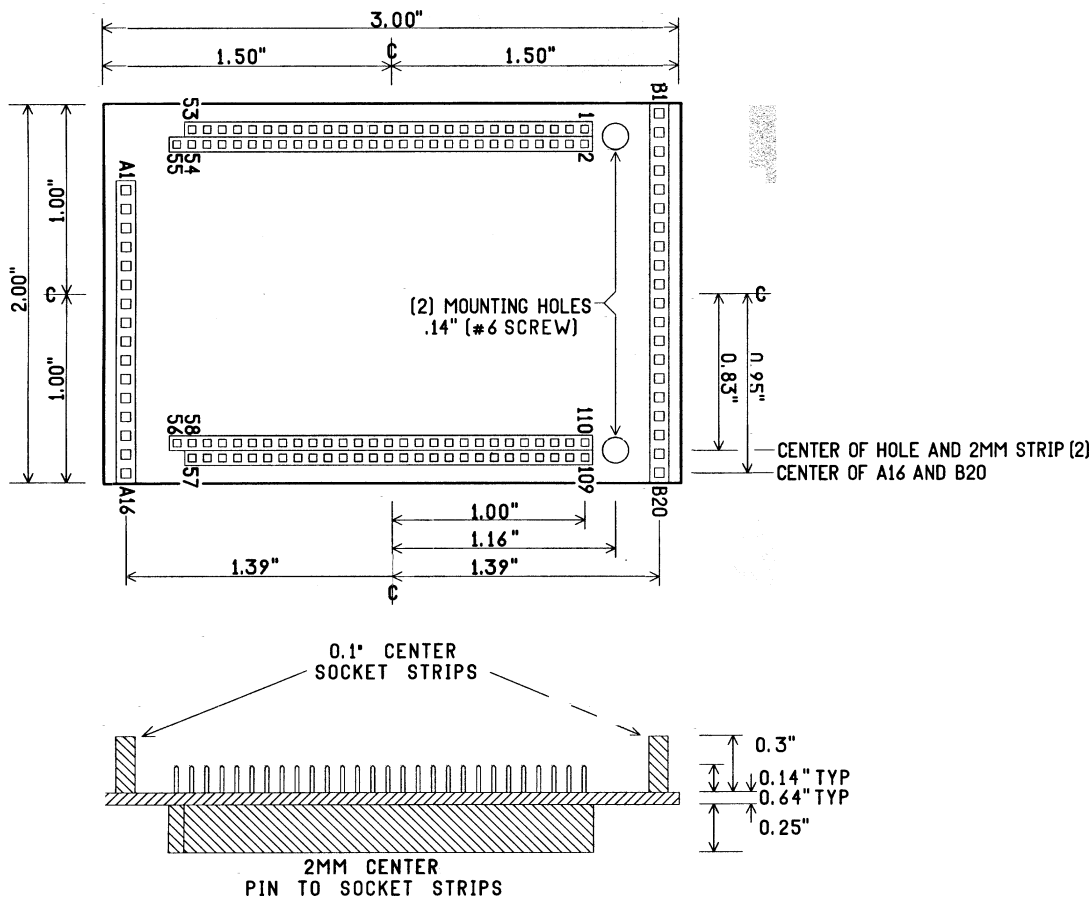
The drawing below gives the dimensions for the TT8-V2 board and the connector positions relative to the board centerlines. Onset Computer Corp has files in electronic format that you can use to help with your layout. Call for details.

ONSET COMPUTER

D-4943-A

LOCATION OF MOUNTING HOLES AND PINS FOR TT8V2

CONNECTORS A AND B ARE 0.1" CENTERS FOR 0.025" SQUARE PINS
 CONNECTORS FOR PINS 1 THROUGH 110 ARE 2MM CENTERS FOR 0.020" SQUARE PINS
 DIMENSIONS OF PIN LOCATIONS ARE TO PIN CENTERS

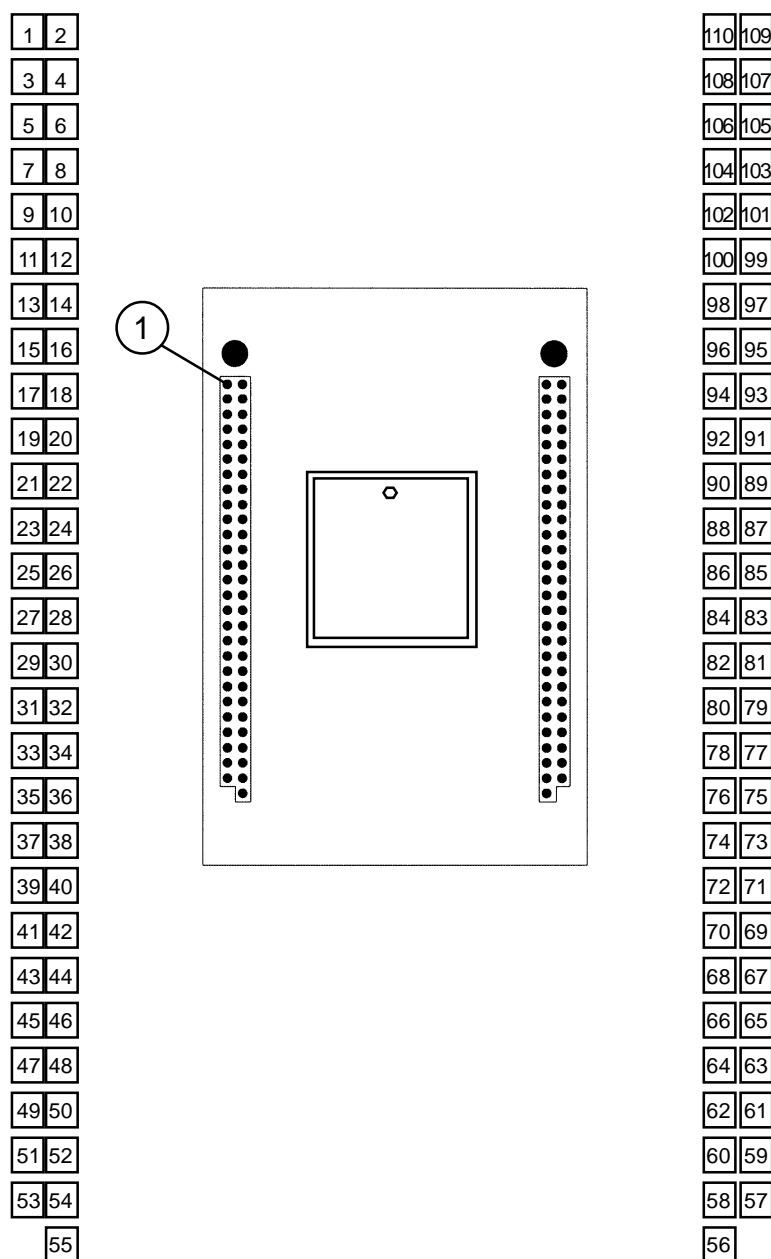


STACKING CONNECTORS

The connectors used are Samtec SQT-127-03-G-S and SQT-128-03-G-S stacking connectors. There are four connectors used for the IIO SquishyBus connections, two each of the Ix27 and Ix28. The I/O-8 connectors were kept for backward compatibility and are described in the [Tattletale Model 8 Installation and Operation Manual](#).

PIN NUMBERING

The pin numbering follows a regular pattern, but it may be a bit confusing. When the board is oriented as below and the CPU is facing you PIN 1 is in the upper left corner. On the left side connector pin numbers increase as you go left to right and down. On the right connector pin numbers increase as you go right to left and up. Just remember that the odd numbered pins are always to the outside of the board, and the even numbered pins are on the inside.



PIN DESIGNATIONS

The figure below shows the pins with a short description of the pin's signal. For a more complete description of each pin's function refer to the [Tattletale Model 8 Installation and Operation Manual](#) or the Motorola manuals..

1	VBAT	Unregulated Supply	110	VREG	Positive supply
2	CLKEN	Clock enable	109	VREF	A/D reference voltage
3	-HEY	Interrupt on change pin	108	AVSS	A/D negative reference
4	-MCLR	Master Clear	107	AD0	A/D channel 0
5	TP12	TPU channel 12	106	AD1	A/D channel 1
6	TP11	TPU channel 11	105	AD2	A/D channel 2
7	TP10	TPU channel 10	104	AD3	A/D channel 3
8	TP9	TPU channel 9	103	AD4	A/D channel 4
9	TP8	TPU channel 8	102	AD5	A/D channel 5
10	TP7	TPU channel 7	101	AD6	A/D channel 6
11	TP6	TPU channel 6	100	AD7	A/D channel 7
12	TP5	TPU channel 5	99	REFADJ	A/D Reference Adjust
13	TP4	TPU channel 4	98	AGND	The analog ground
14	TP3	TPU channel 3	97	SEL5V	Clock mode select
15	TP2	TPU channel 2	96	RSR2	RS-232 receive (jack 2)
16	TP1	TPU channel 1	95	RST2	RS-232 transmit (jack 2)
17	TP0	TPU channel 0	94	RSR1	RS-232 receive (jack 1)
18	TXD2	TPU UART transmit	93	RST1	RS-232 transmit (jack 1)
19	RXD2	TPU UART receive	92	ECLK	Outputs 1/8 SYSCLK or -CS3
20	TP15	TPU channel 15	91	-CS2	Chip select
21	T2CLK	TPU clock in	90	-CS1	Chip select
22	A1	CPU Address Line	89	-CS0	Chip select
23	A2	CPU Address Line	88	D0	CPU Data Line (D0)
24	A3	CPU Address Line	87	D1	CPU Data Line (D1)
25	A4	CPU Address Line	86	D2	CPU Data Line (D2)
26	A5	CPU Address Line	85	D3	CPU Data Line (D3)
27	A6	CPU Address Line	84	D4	CPU Data Line (D4)
28	A7	CPU Address Line	83	D5	CPU Data Line (D5)
29	A8	CPU Address Line	82	D6	CPU Data Line (D6)
30	A9	CPU Address Line	81	D7	CPU Data Line (D7)
31	A10	CPU Address Line	80	D8	CPU Data Line (D8)
32	A11	CPU Address Line	79	D9	CPU Data Line (D9)
33	A12	CPU Address Line	78	D10	CPU Data Line (D10)
34	A13	CPU Address Line	77	D11	CPU Data Line (D11)
35	A14	CPU Address Line	76	D12	CPU Data Line (D12)
36	A15	CPU Address Line	75	D13	CPU Data Line (D13)
37	A16	CPU Address Line	74	D14	CPU Data Line (D14)
38	A17	CPU Address Line	73	D15	CPU Data Line (D15)
39	A18	CPU Address Line	72	A0	CPU Address Line (A0)
40	A19	CPU Address Line	71	E4	Port E
41	MISO	Master-In Slave-Out (QSPI)	70	E3	Port E
42	MOSI	Master-Out Slave-In (QSPI)	69	E2	Port E
43	SCK	QSPI serial clock	68	E1	Port E
44	PCS0	QSPI chip select	67	E0	Port E
45	PCS1	QSPI chip select	66	E5	Port E
46	PCS2	QSPI chip select	65	E6	Port E
47	PCS3	QSPI chip select	64	E7	Port E
48	DSI	Development serial in	63	R/-W	Read/Write
49	DSO	Development serial out	62	-IRQ2	Interrupt request (level 2)
50	RXD1	SCI receive data	61	-IRQ3	Interrupt request (level 3)
51	TXD1	SCI transmit data	60	-IRQ4	Interrupt request (level 4)
52	DSCLK	Development serial clock	59	-PICIRQ	Interrupt request
53	-FRZ	Freeze	58	40KHZ	40KHz clock out
54	-RESET	Reset	57	RSDIS	RS-232 driver disable
55	DGND	Digital Ground	56	CLKOUT	

THE PR8-V2 BREADBOARD

The PR8-V2 breadboard was designed to provide all the connections available on the original PR8 and support more additional expansion features than before, but in a smaller size. The board is designed to fit inside a standard SERPAC enclosure style A-27.

